

FIG. 1

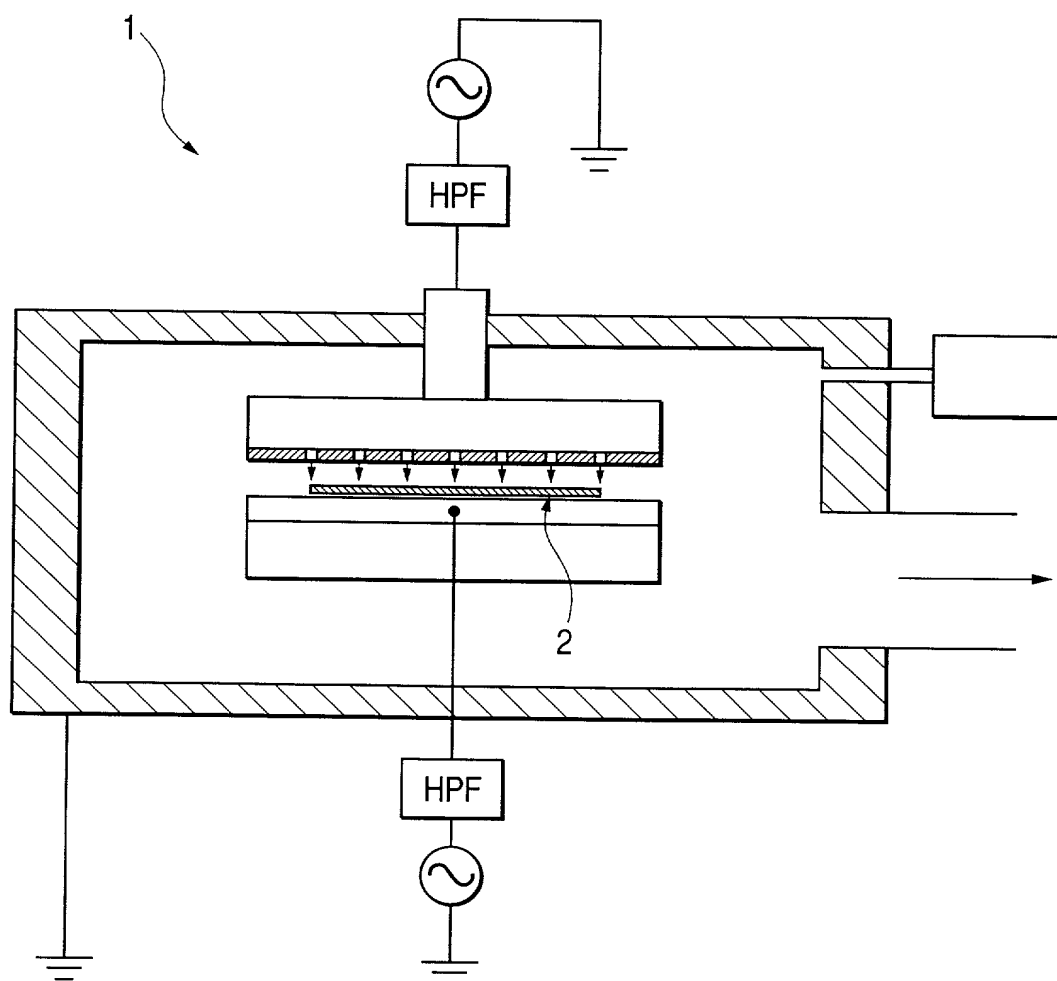
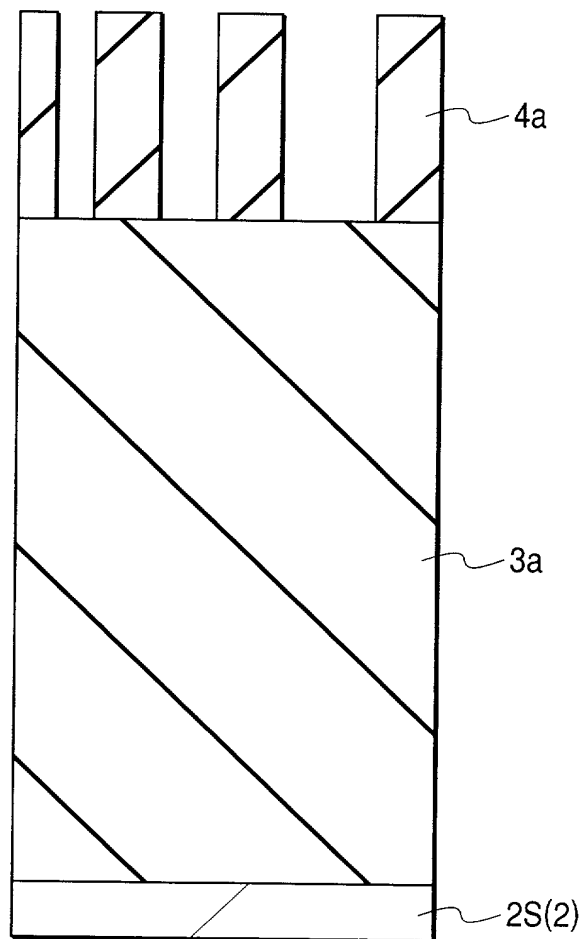


FIG. 2



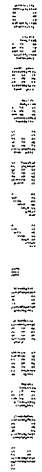
[illegible]

FIG. 4(a)

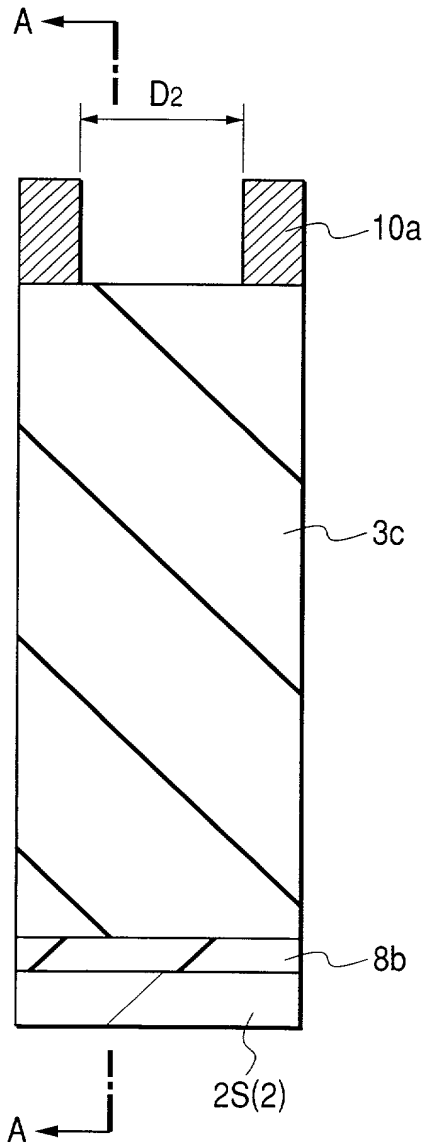


FIG. 4(b)

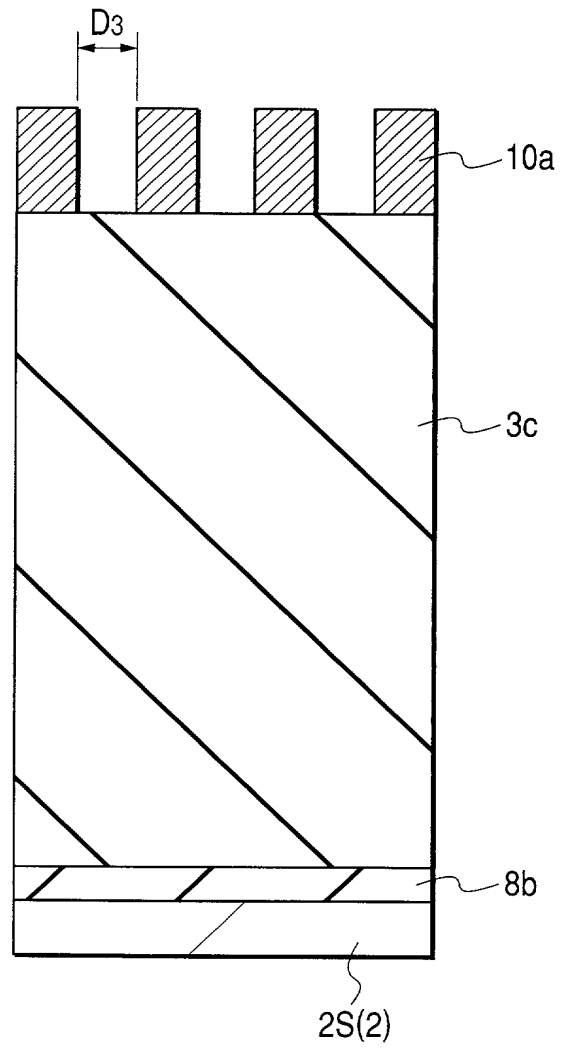


FIG. 5

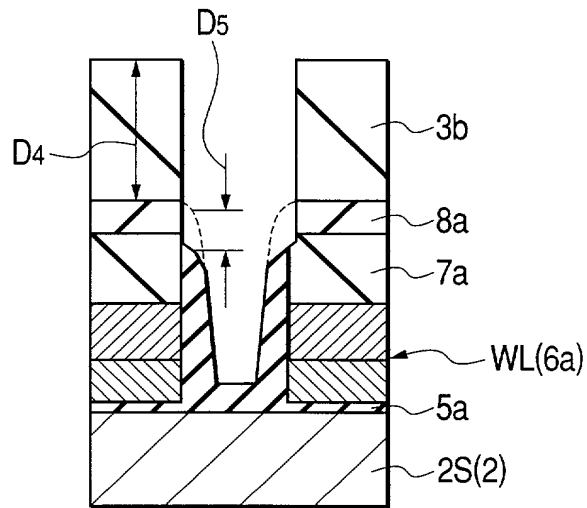


FIG. 6

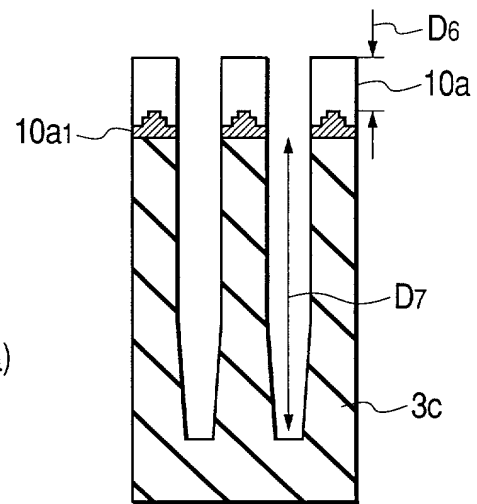


FIG. 7

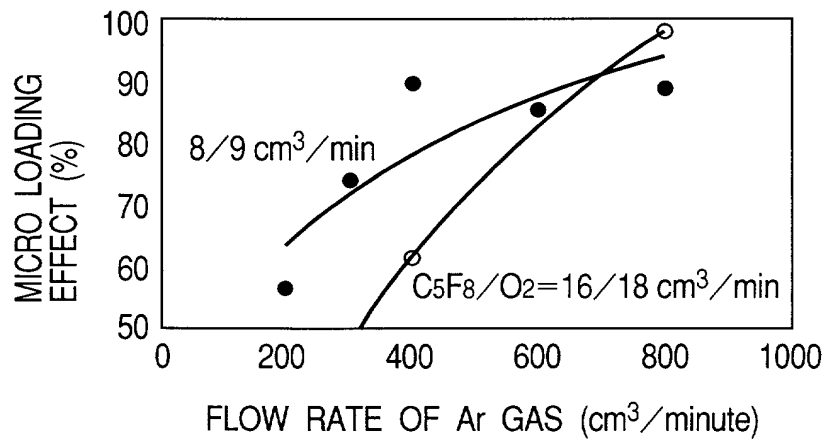


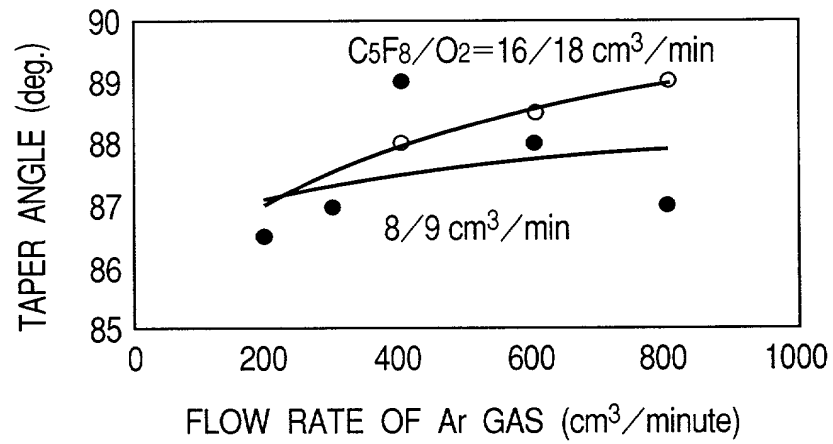
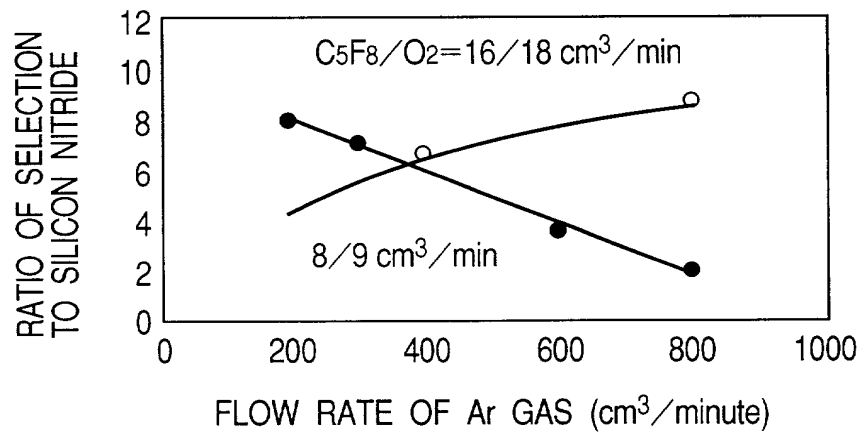
FIG. 8(a)*FIG. 8(b)*

FIG. 9(a)

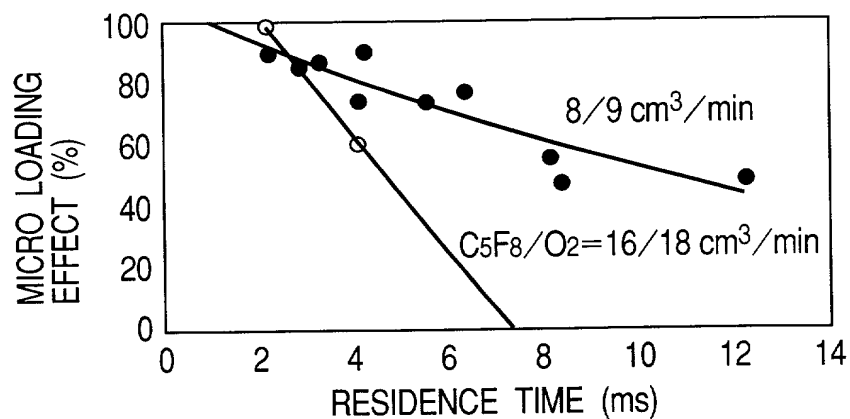


FIG. 9(b)

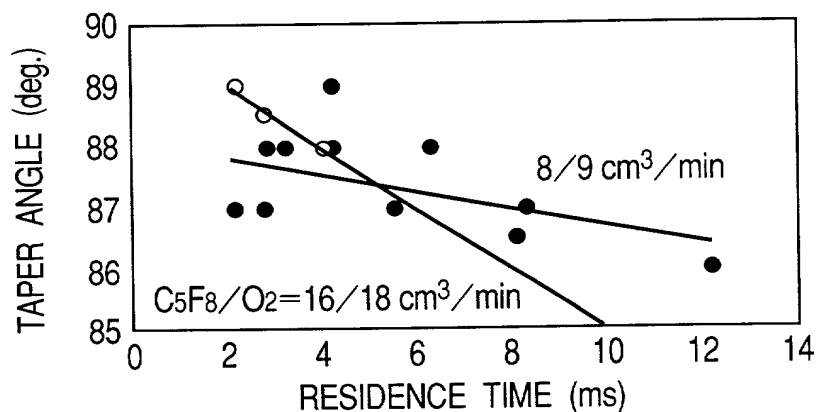
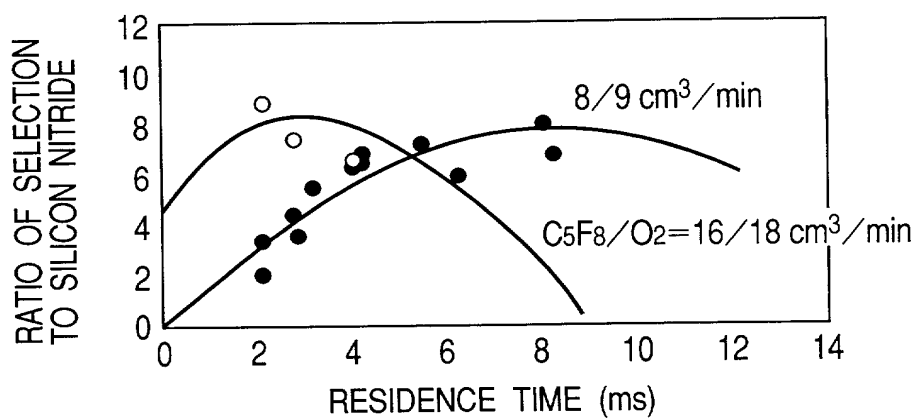


FIG. 9(c)



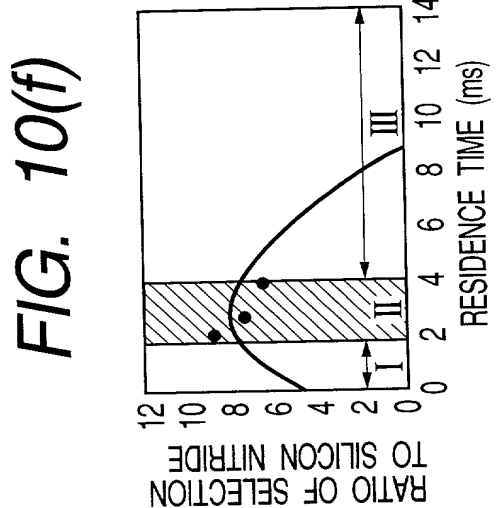
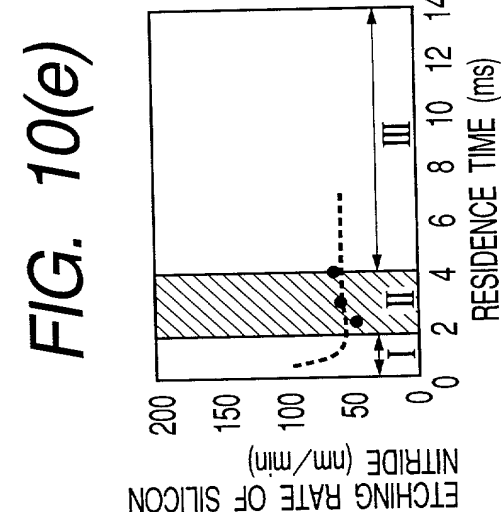
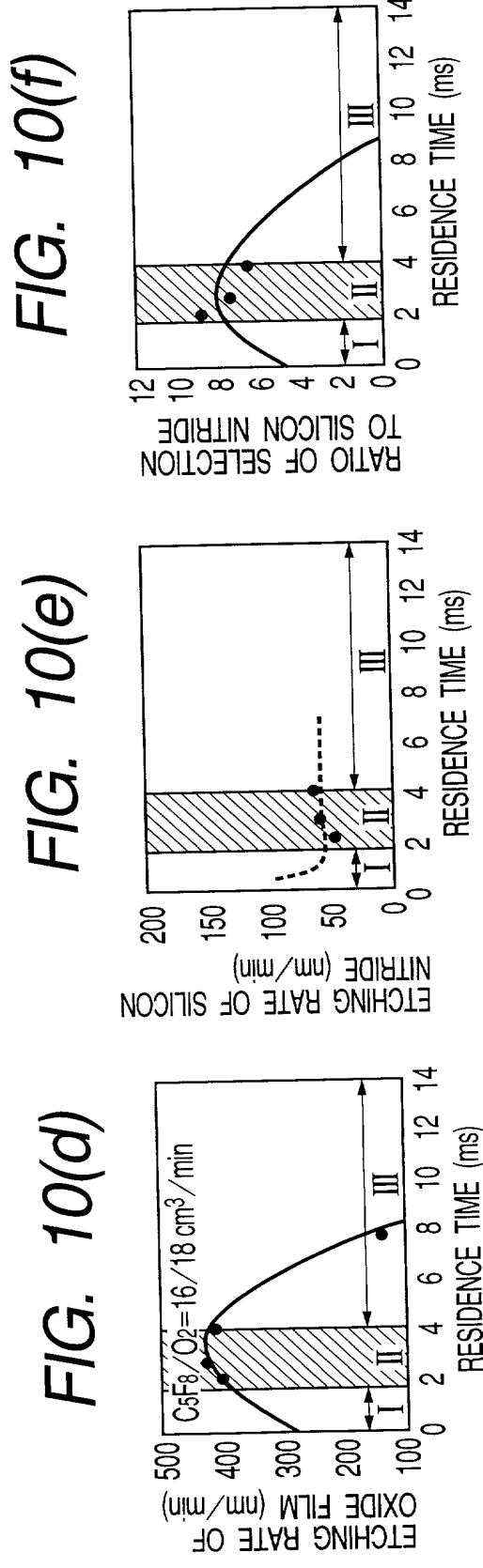
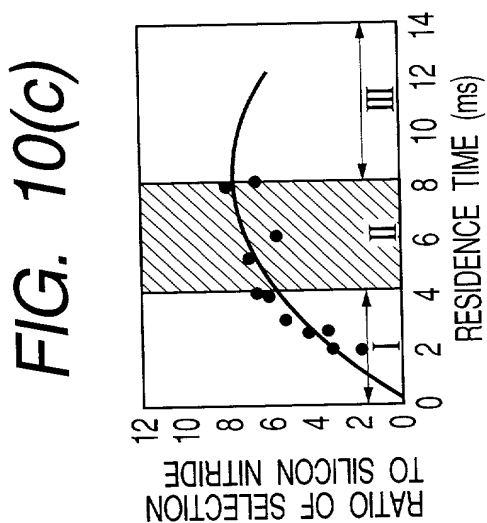
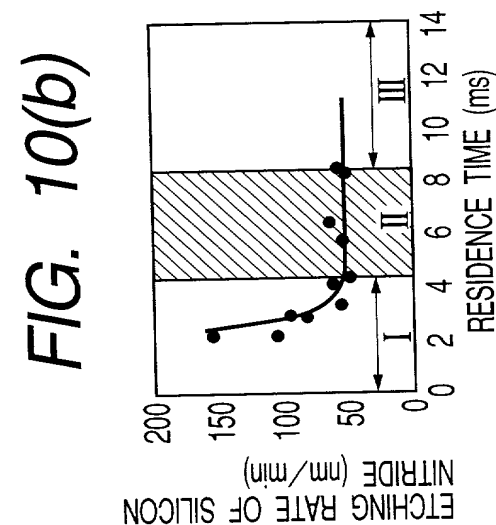
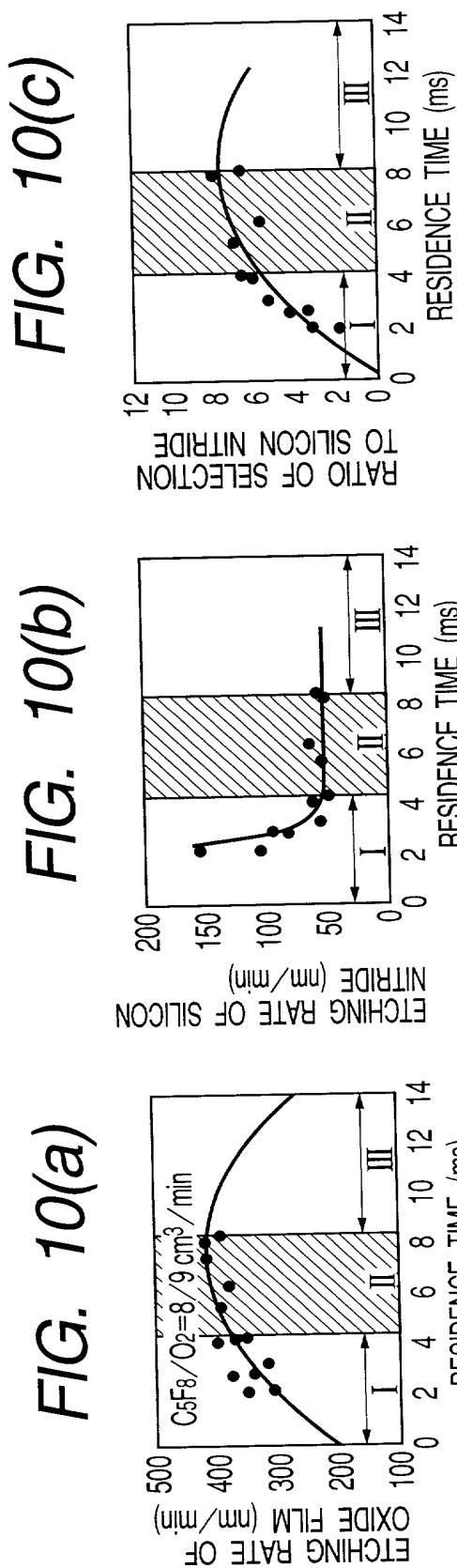


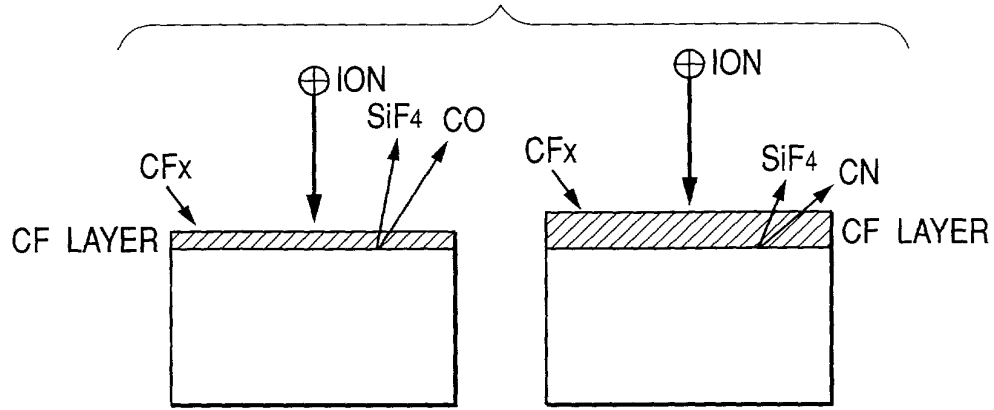
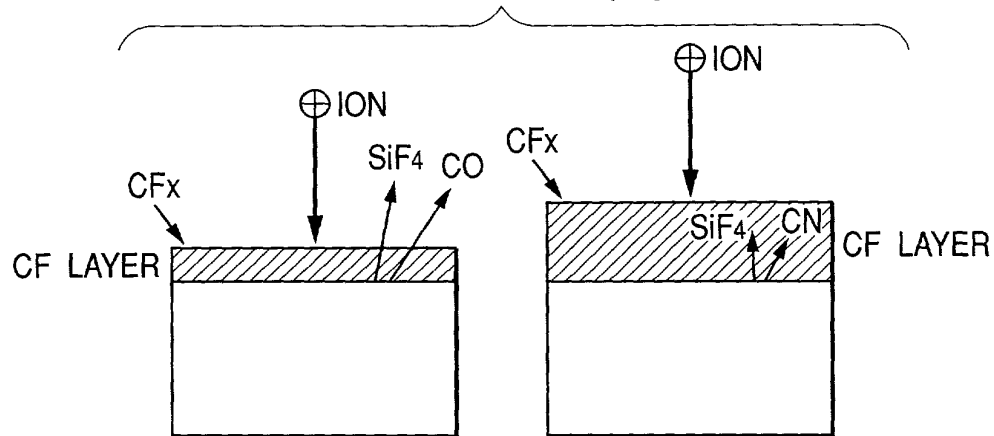
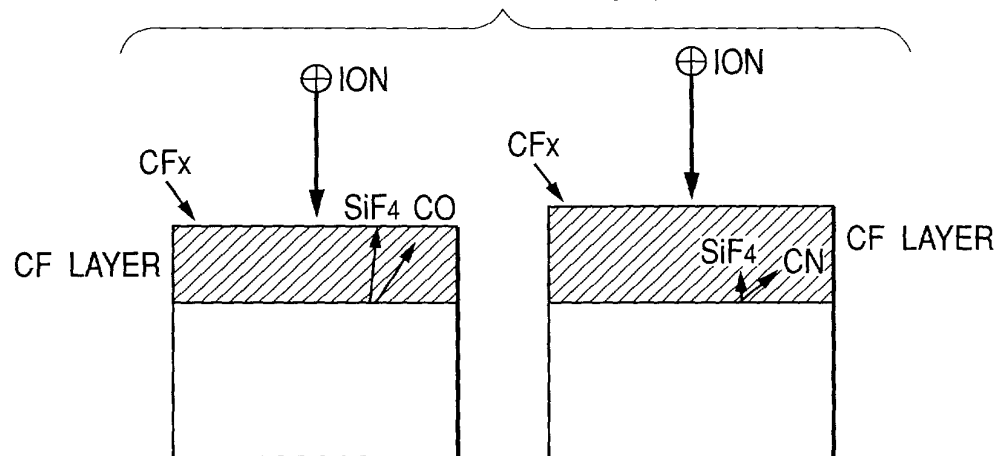
FIG. 11(a)**FIG. 11(b)****FIG. 11(c)**

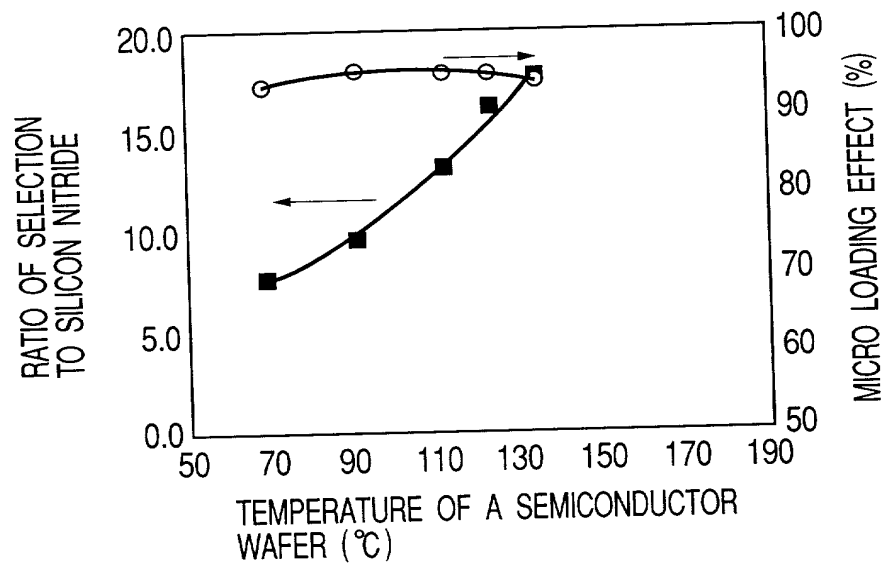
FIG. 12

FIG. 13

PARAMETERS			
PRESSURE	[Pa]		2.66
RF POWER	UPPER PORTION	[W]	800
	LOWER PORTION	[W]	700
FLOW RATE OF C ₅ F ₈	[cm ³ /minute]		16
FLOW RATE OF O ₂	[cm ³ /minute]		18
FLOW RATE OF Ar	[cm ³ /minute]		800
ELECTRODE TEMPERATURE			
	UPPER PORTION	(°C)	60
	LOWER PORTION	(°C)	20
TEMPERATURE OF WALL SURFACE	[°C]		50
ELECTRODE GAP	[mm]		21

FIG. 14

PARAMETERS			
PRESSURE	[Pa]		2.66
RF POWER	UPPER PORTION	[W]	1800
	LOWER PORTION	[W]	1500
FLOW RATE OF C ₅ F ₈	[cm ³ /minute]		24
FLOW RATE OF O ₂	[cm ³ /minute]		28
FLOW RATE OF Ar	[cm ³ /minute]		700
ELECTRODE TEMPERATURE			
	UPPER PORTION	(°C)	60
	LOWER PORTION	(°C)	20
TEMPERATURE OF WALL SURFACE	[°C]		50
ELECTRODE GAP	[mm]		19

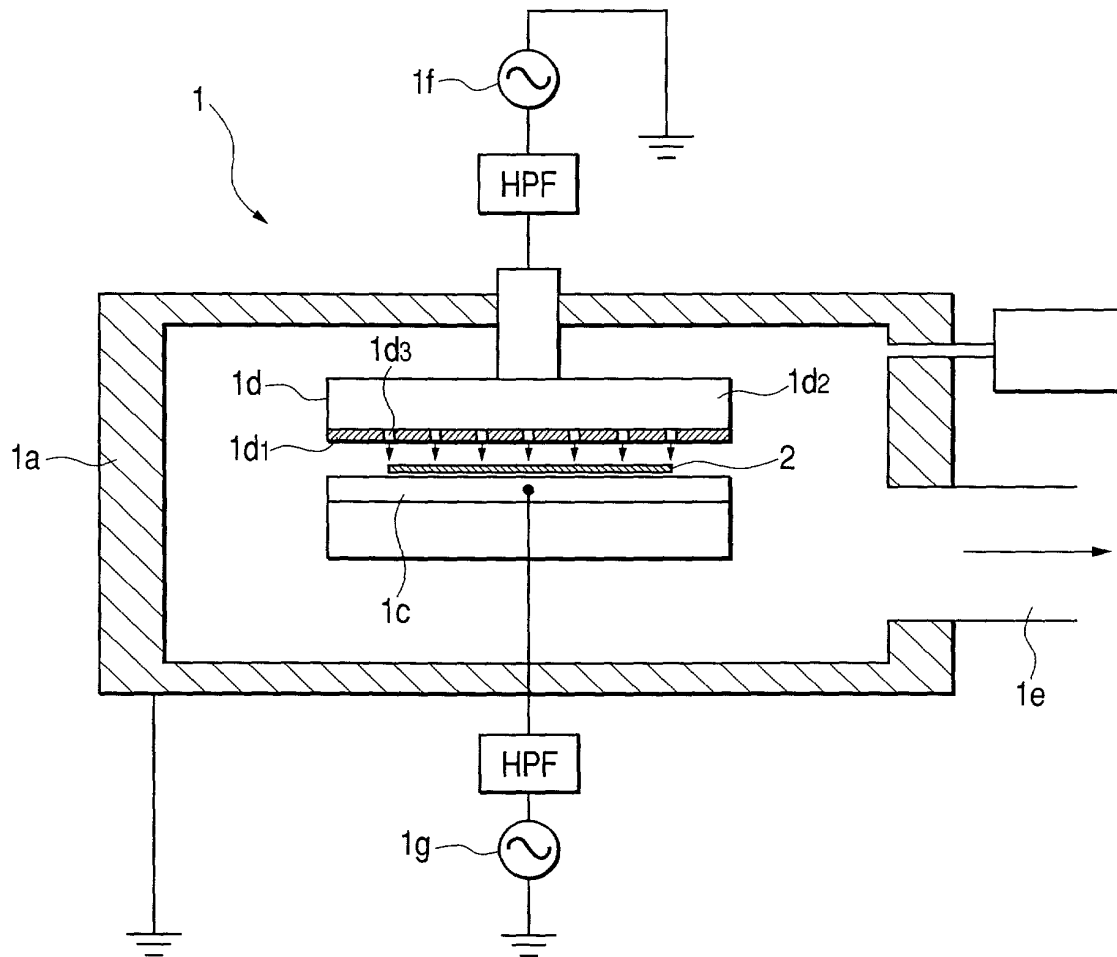
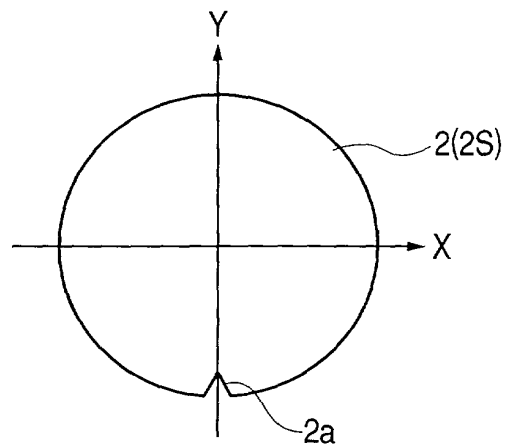
FIG. 15**FIG. 16**

FIG. 17

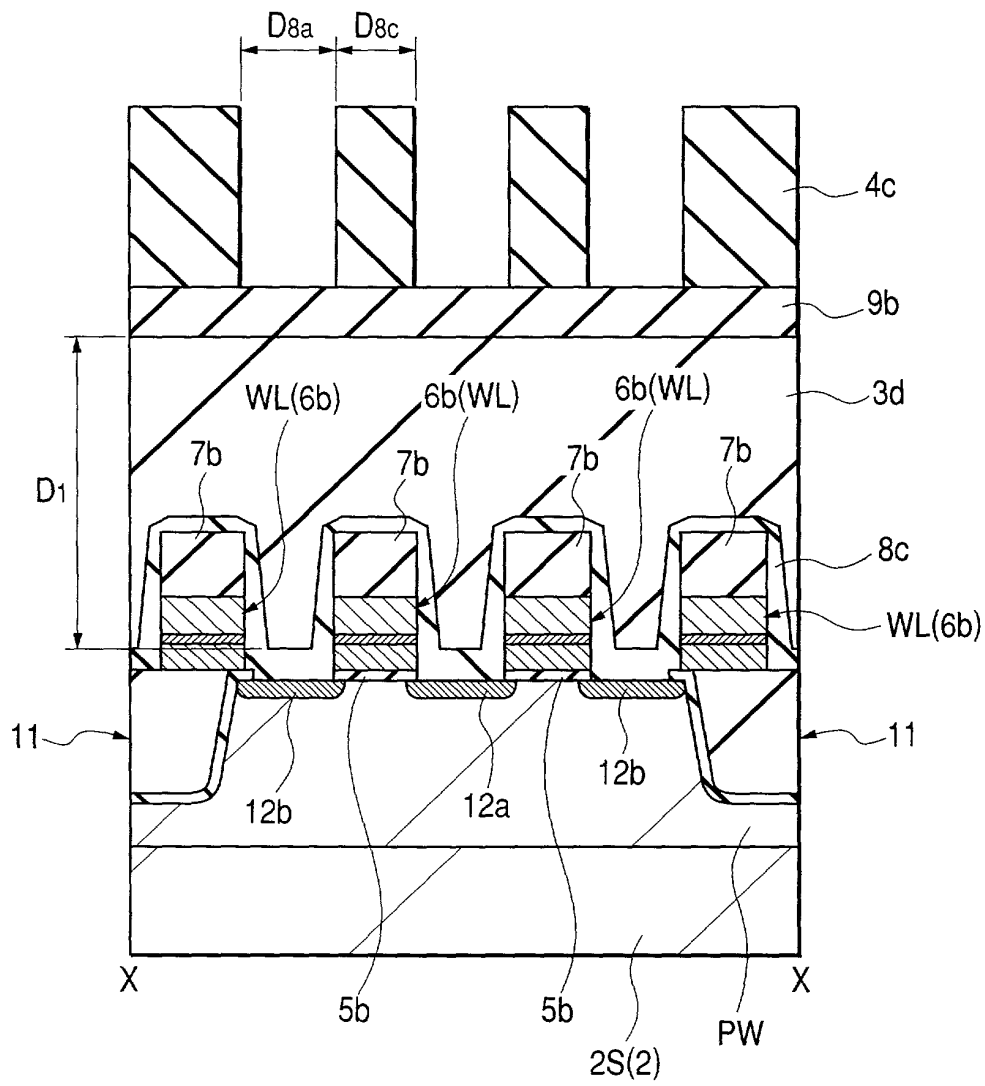


FIG. 18

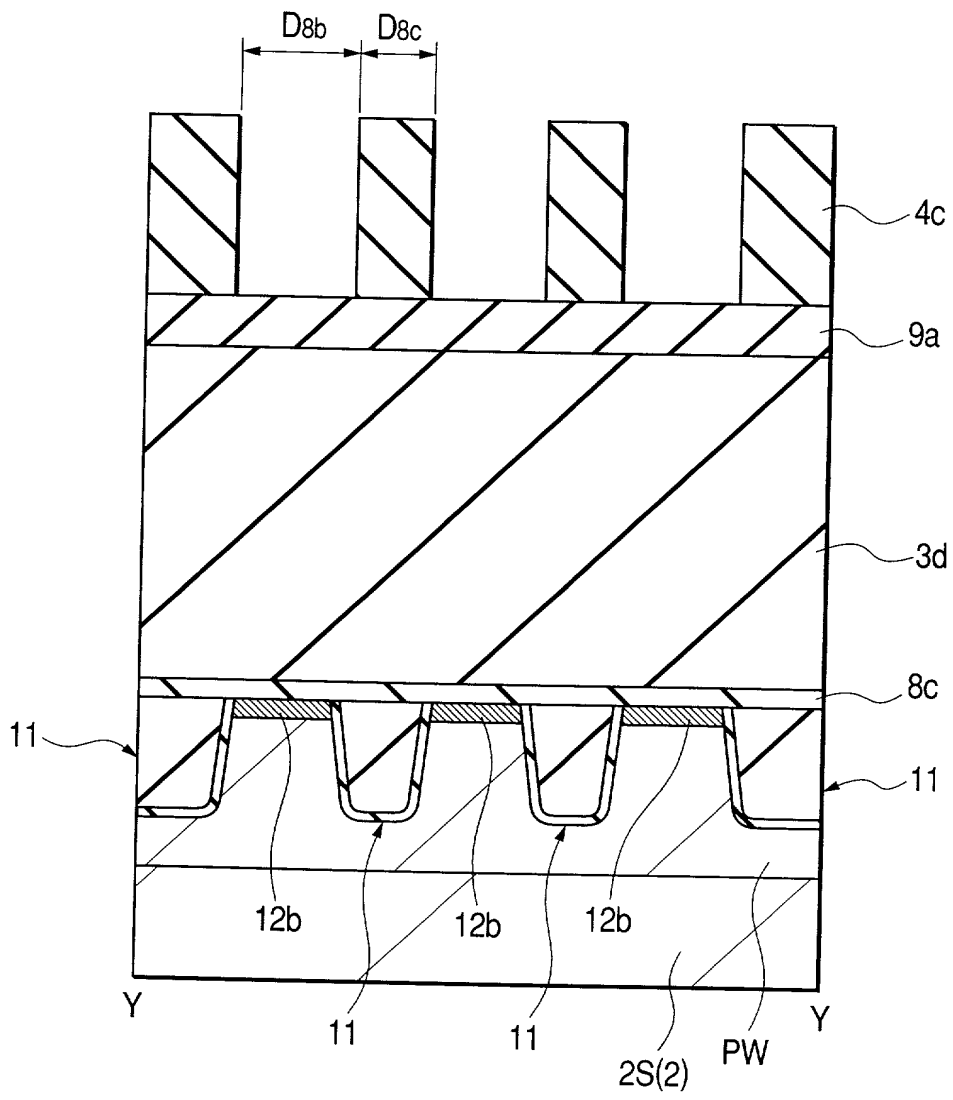


FIG. 19

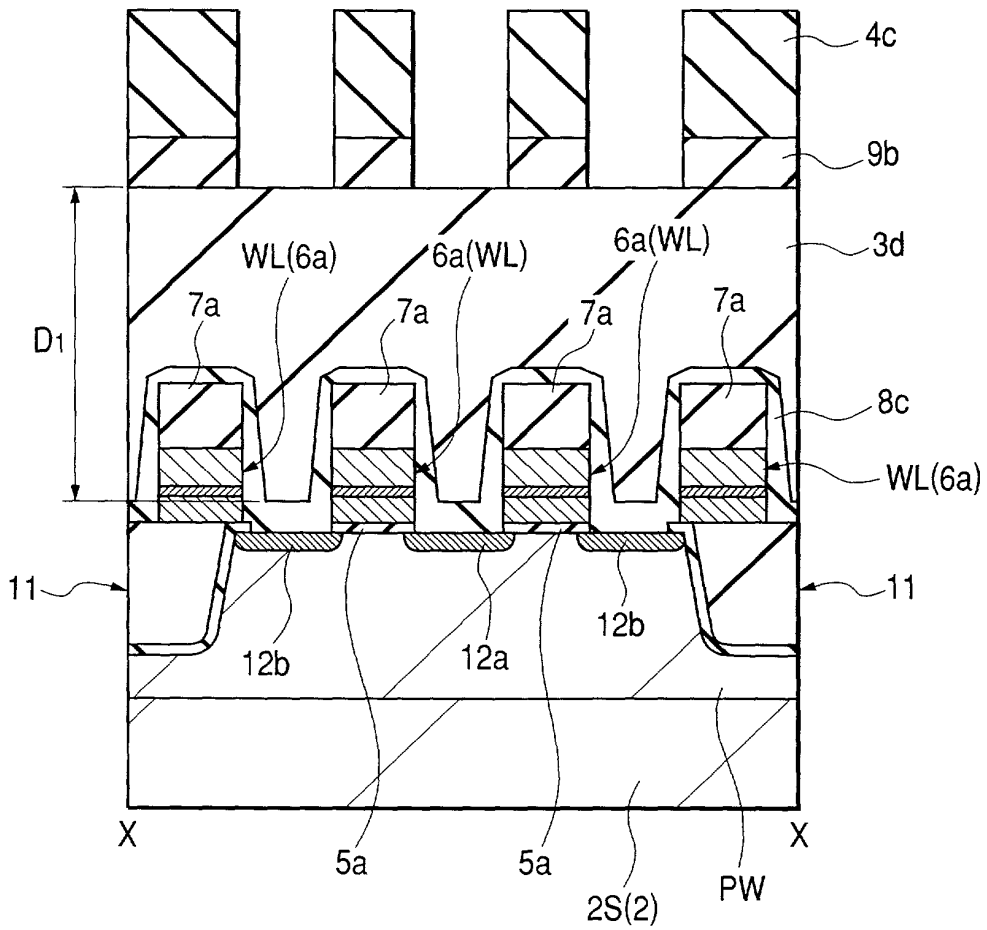


FIG. 20

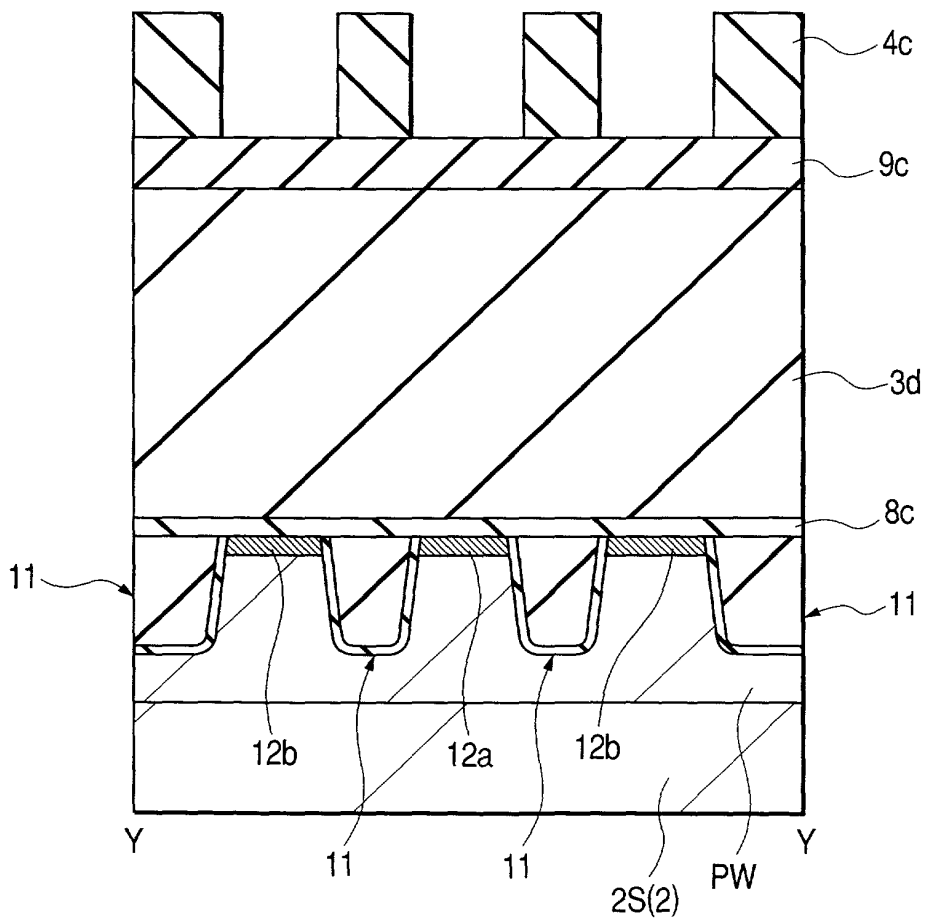


FIG. 21

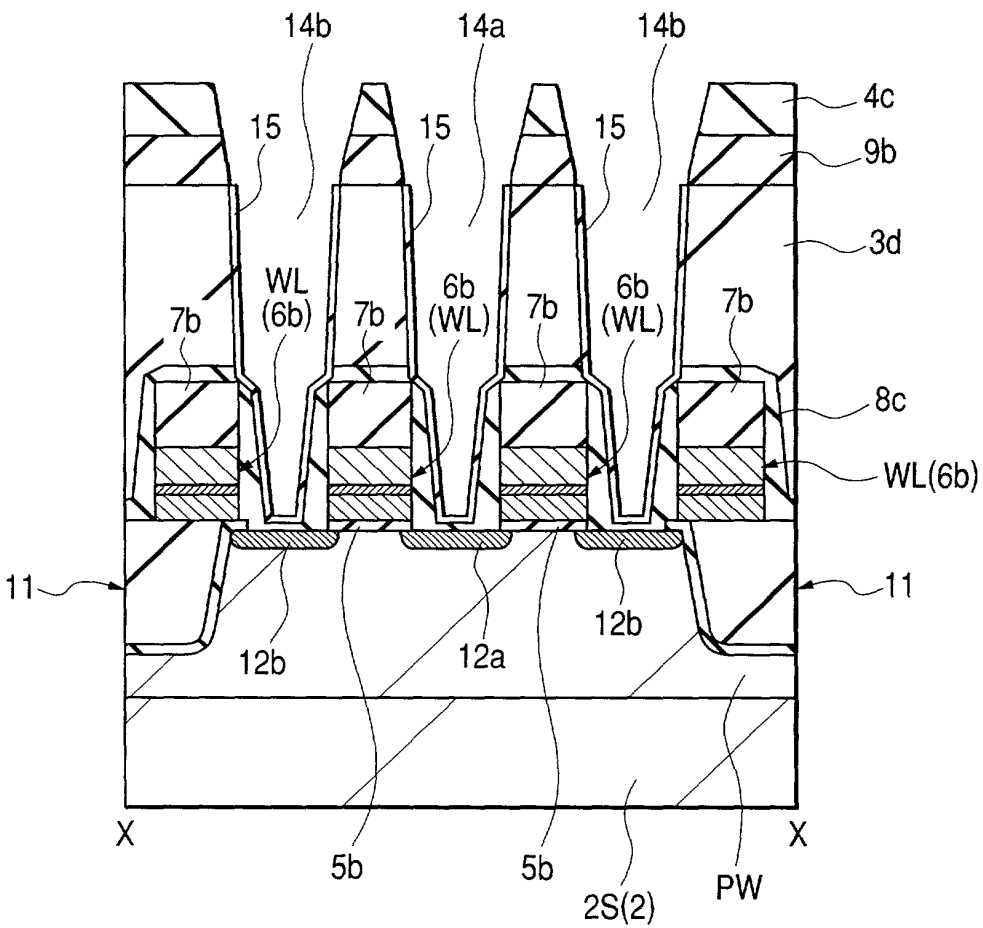


FIG. 22

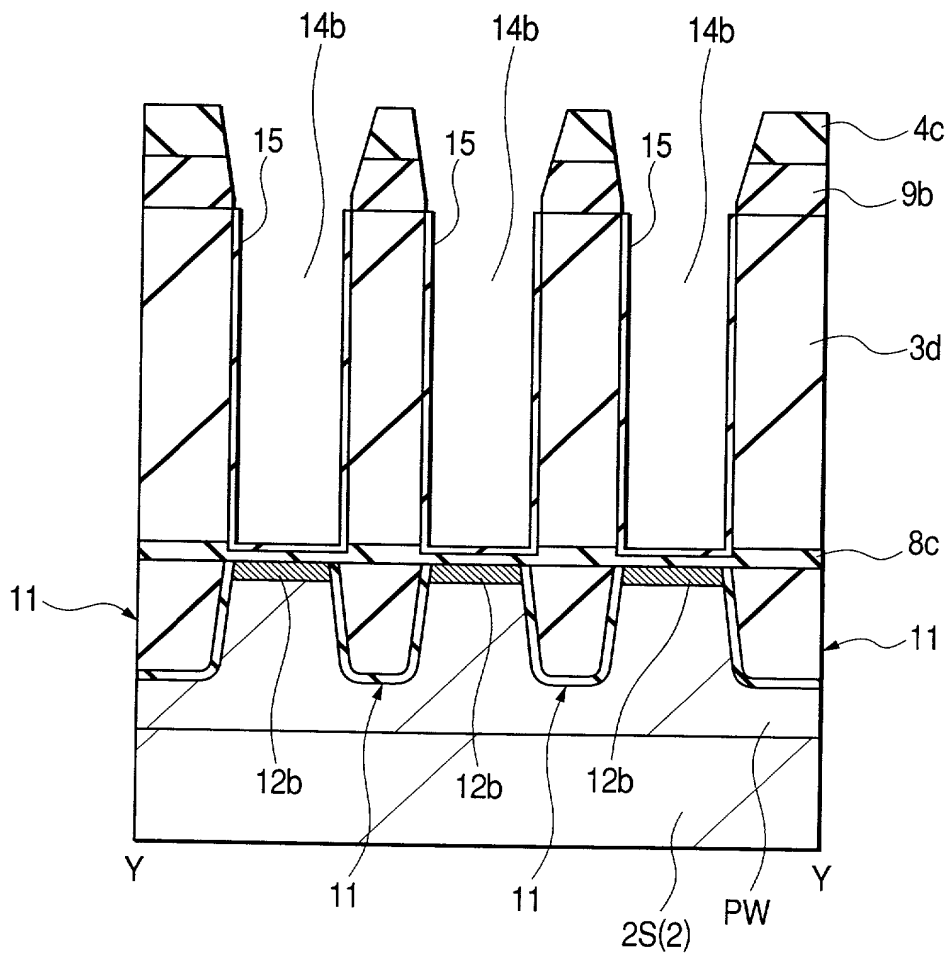


FIG. 23

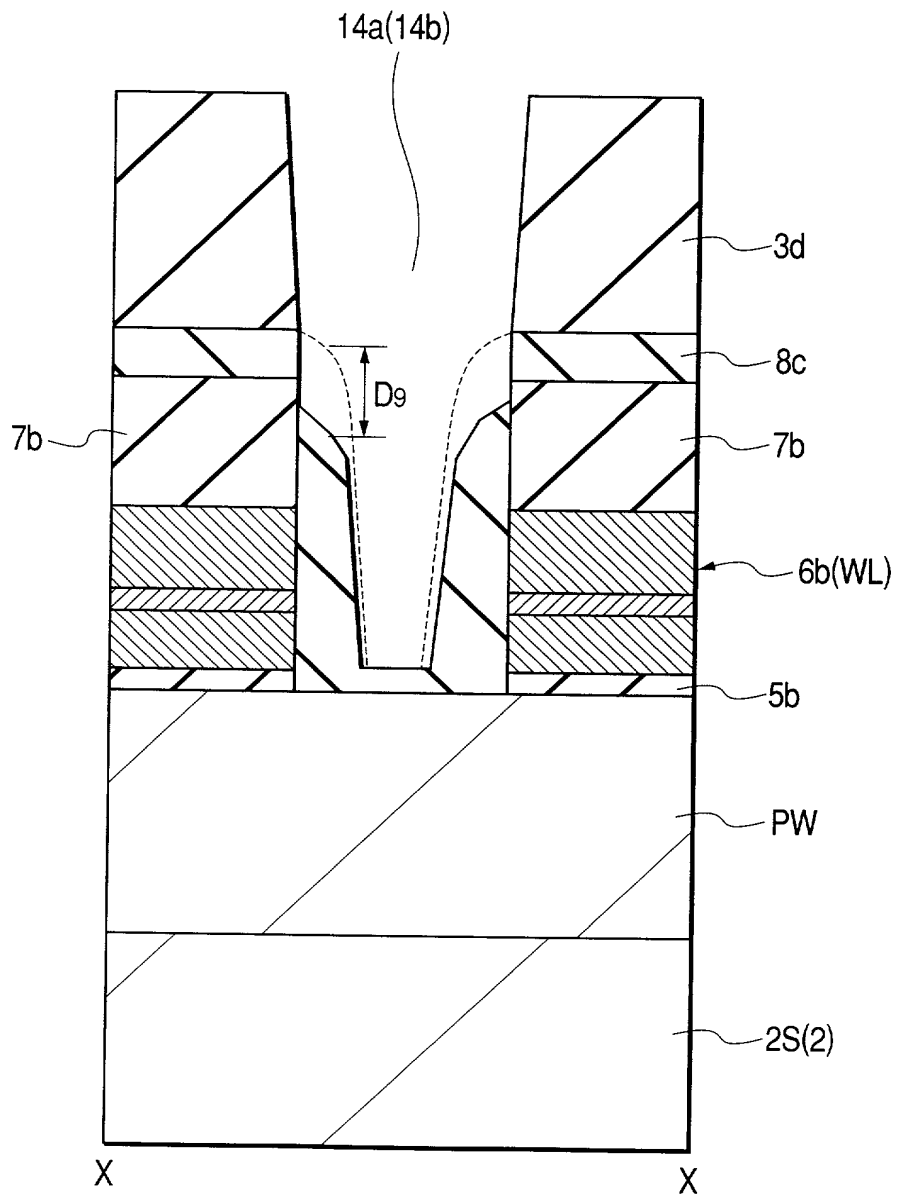


FIG. 24

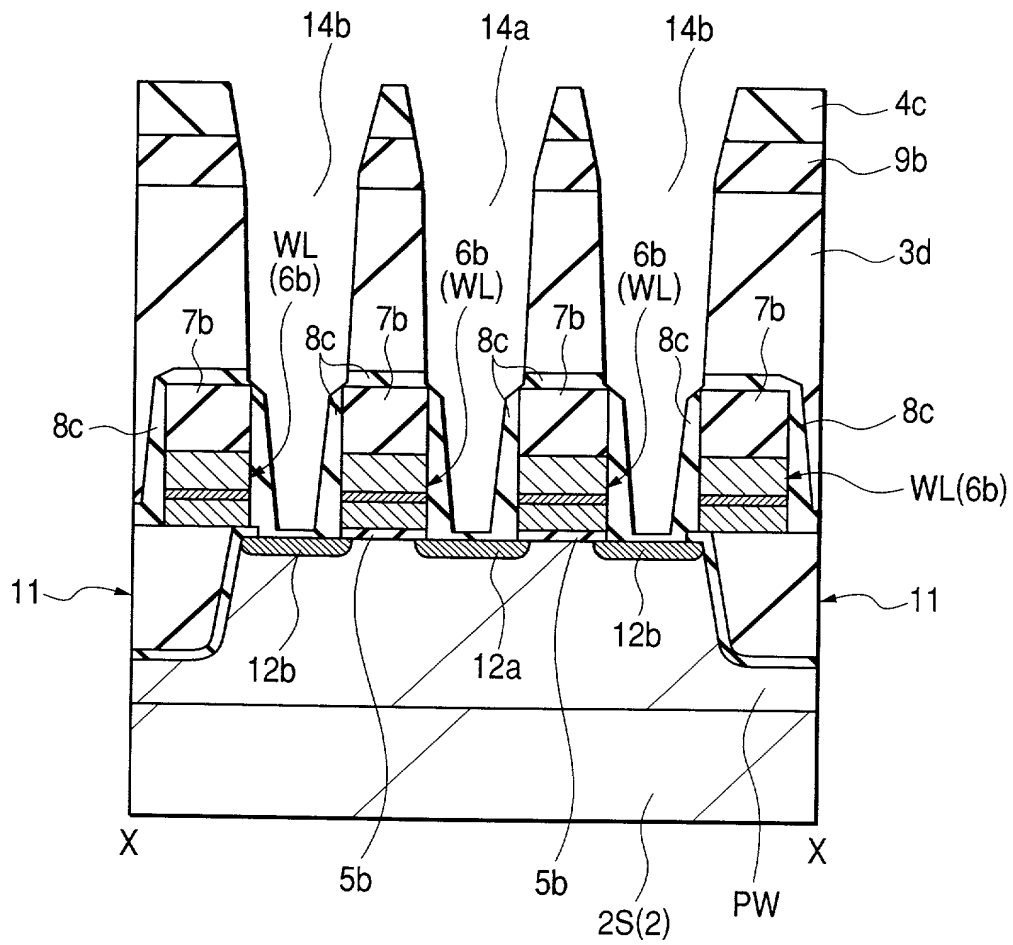


FIG. 25

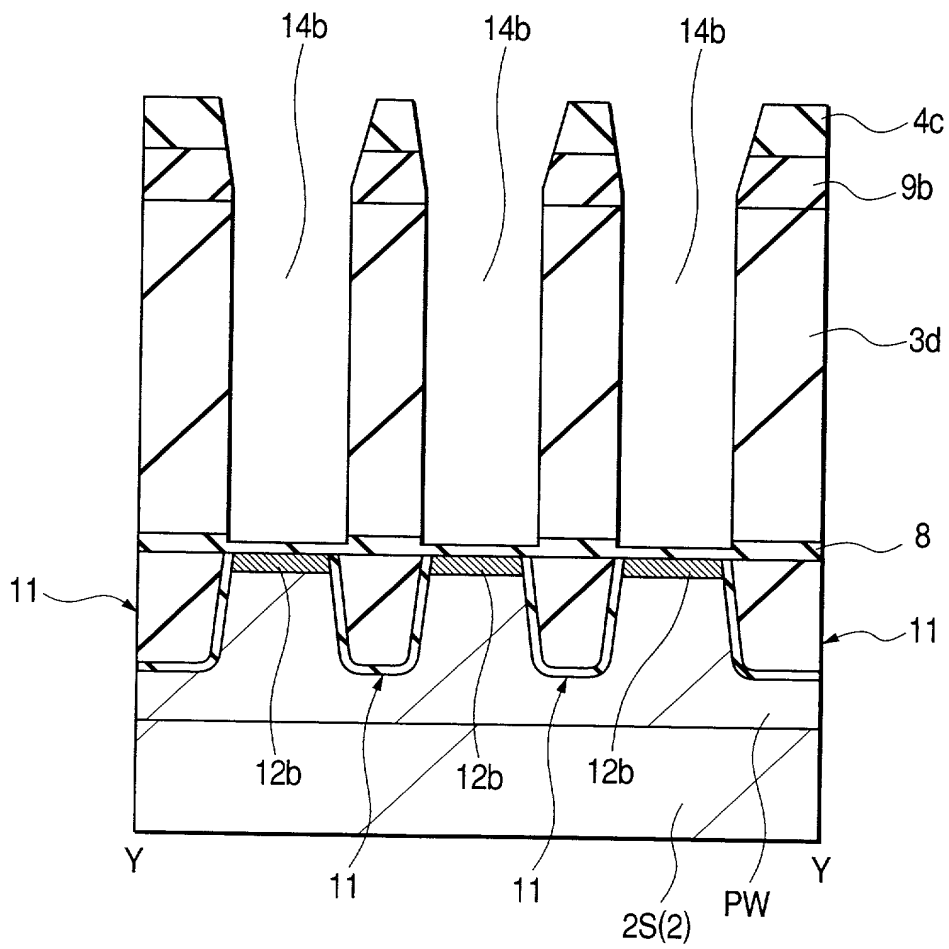


FIG. 26

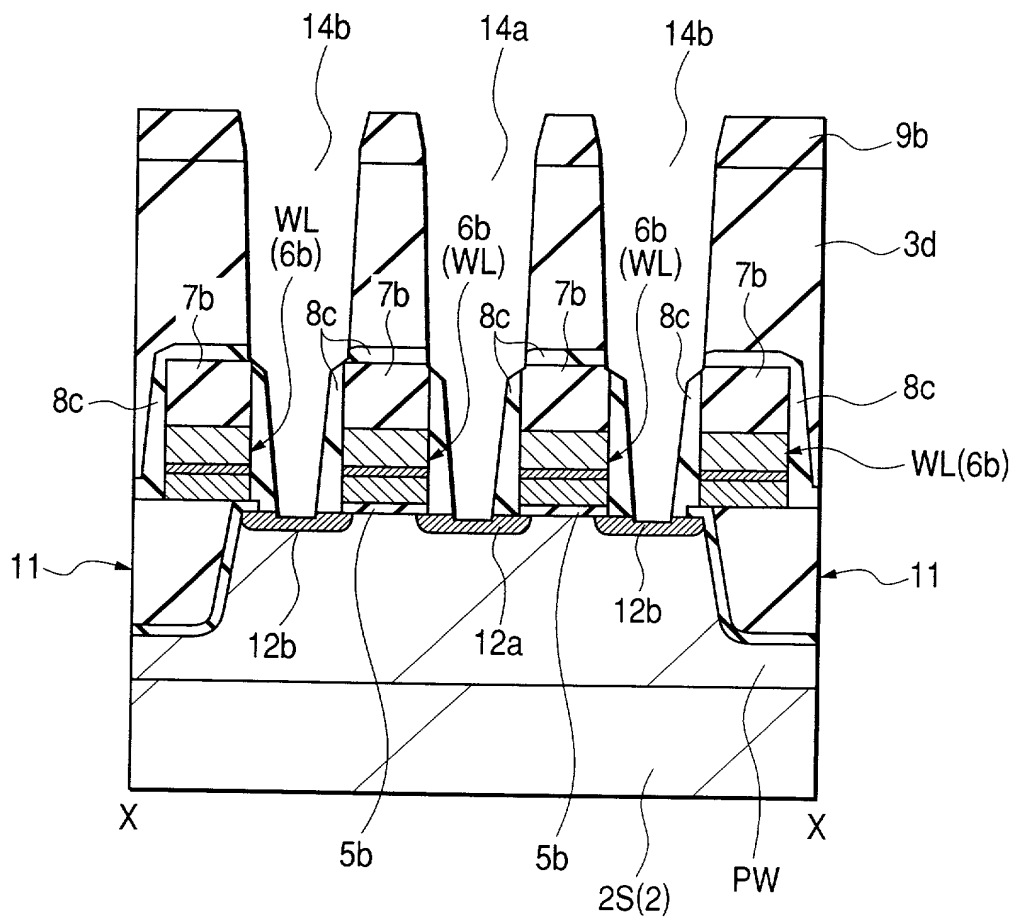


FIG. 27

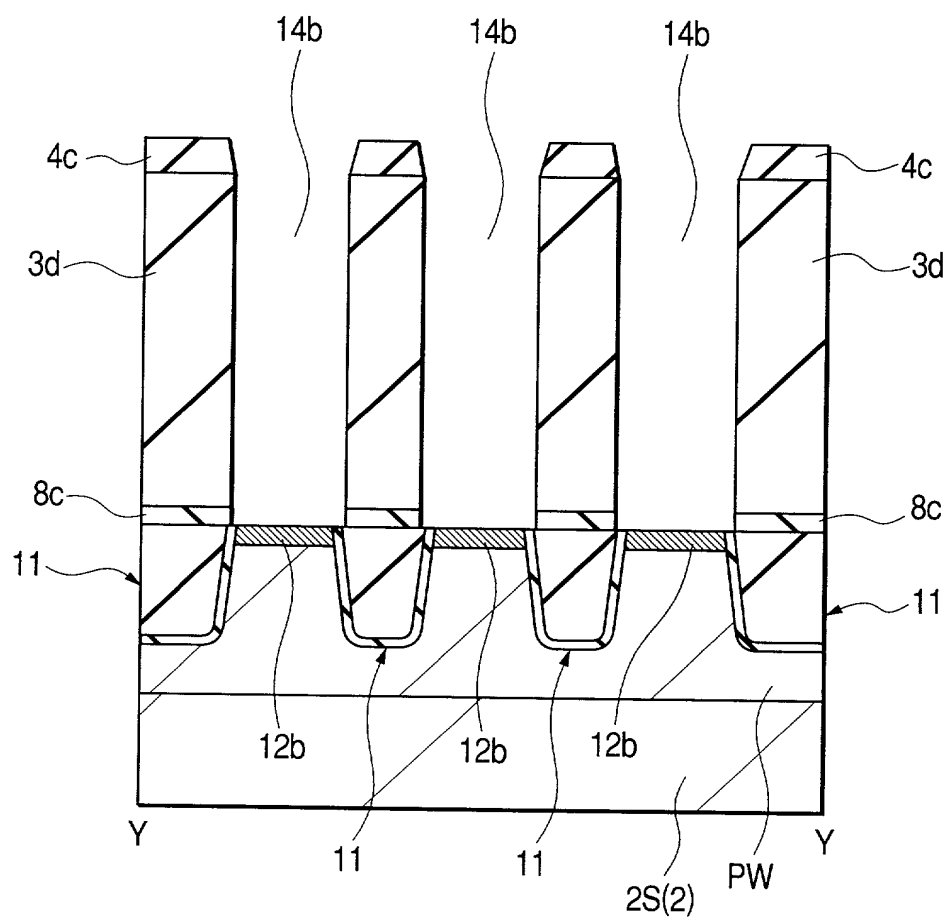


FIG. 28

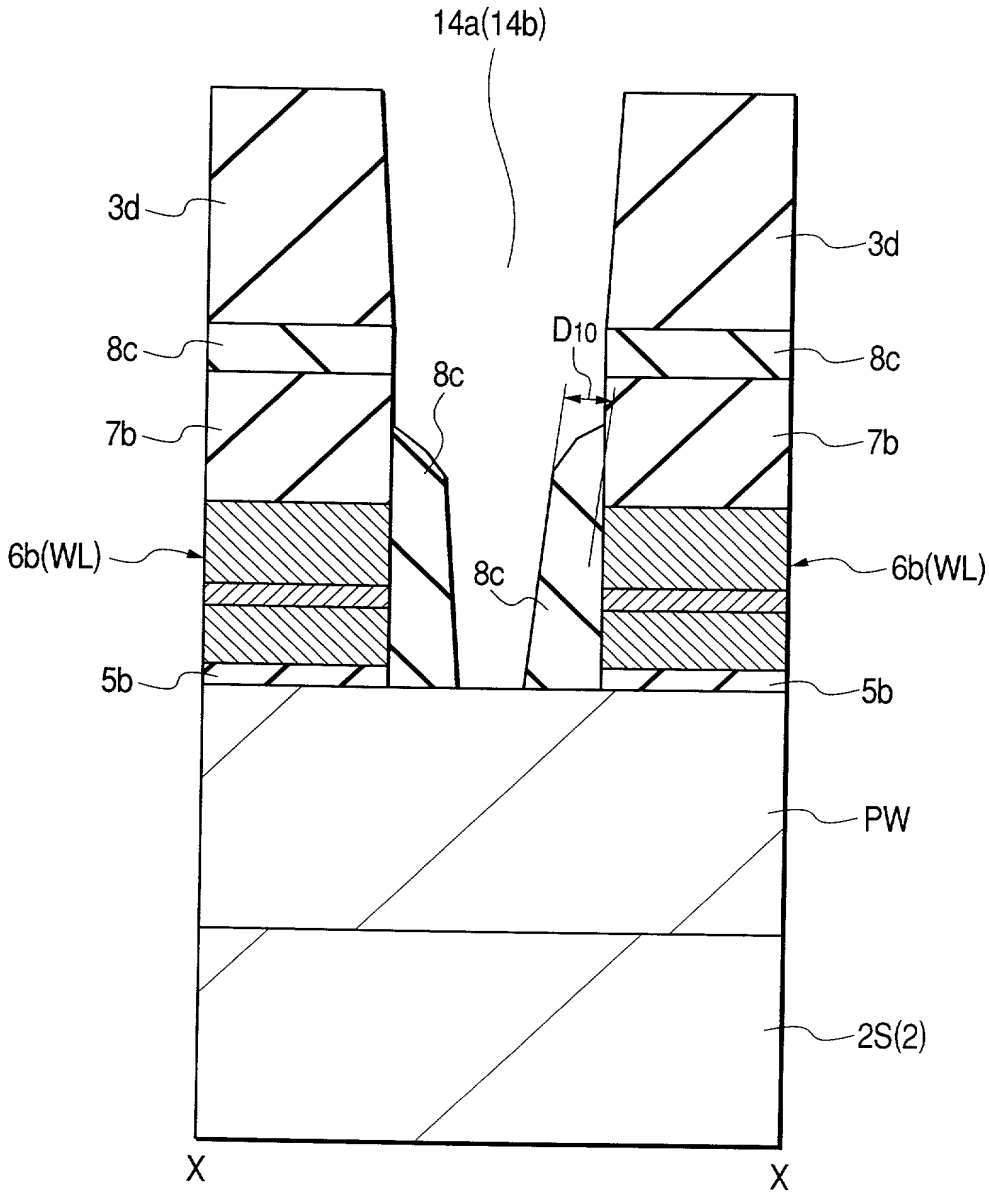


FIG. 29

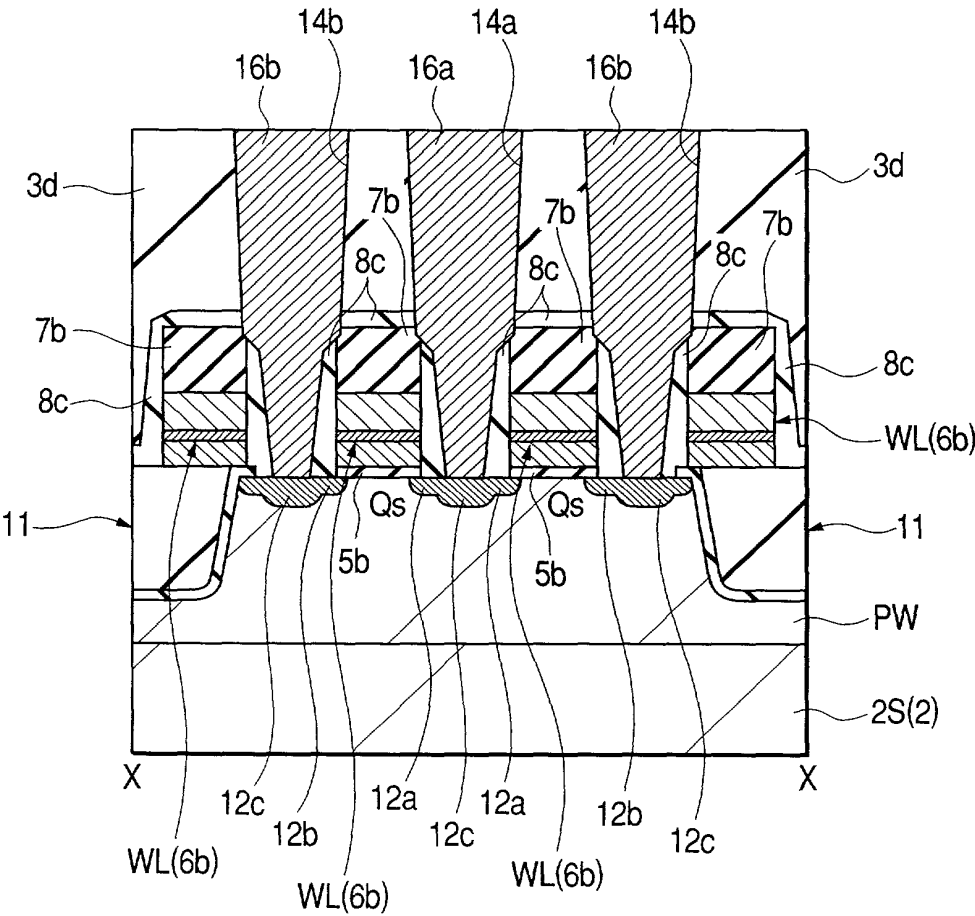


FIG. 30

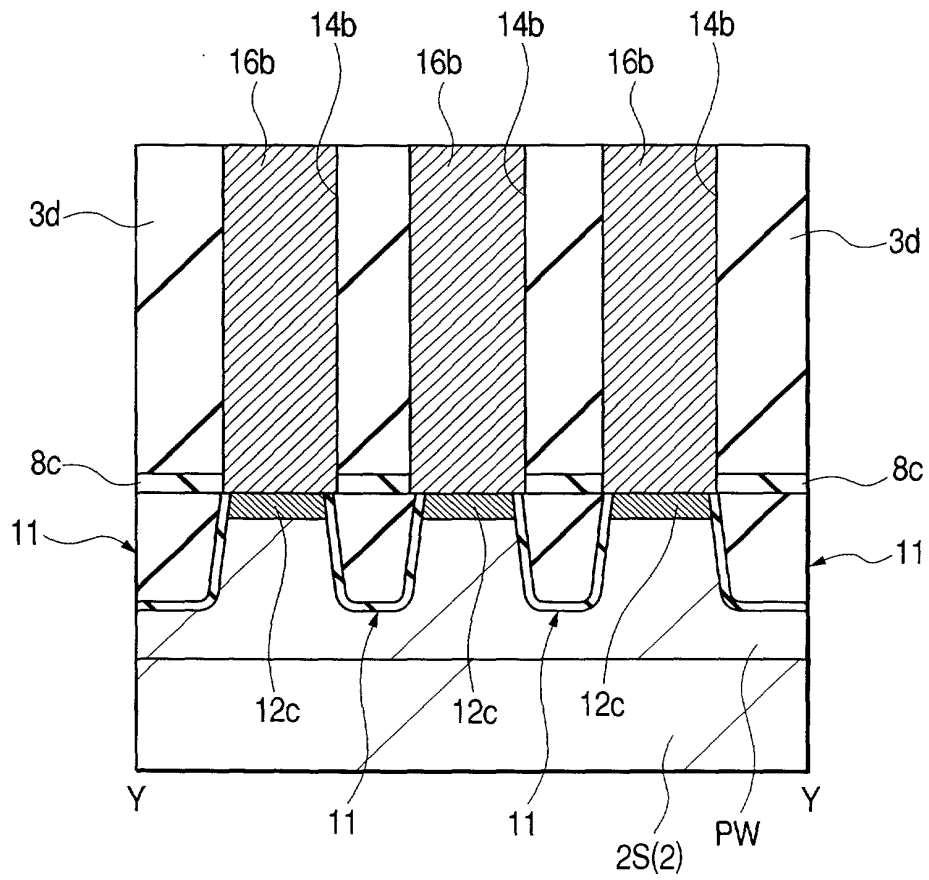


FIG. 31

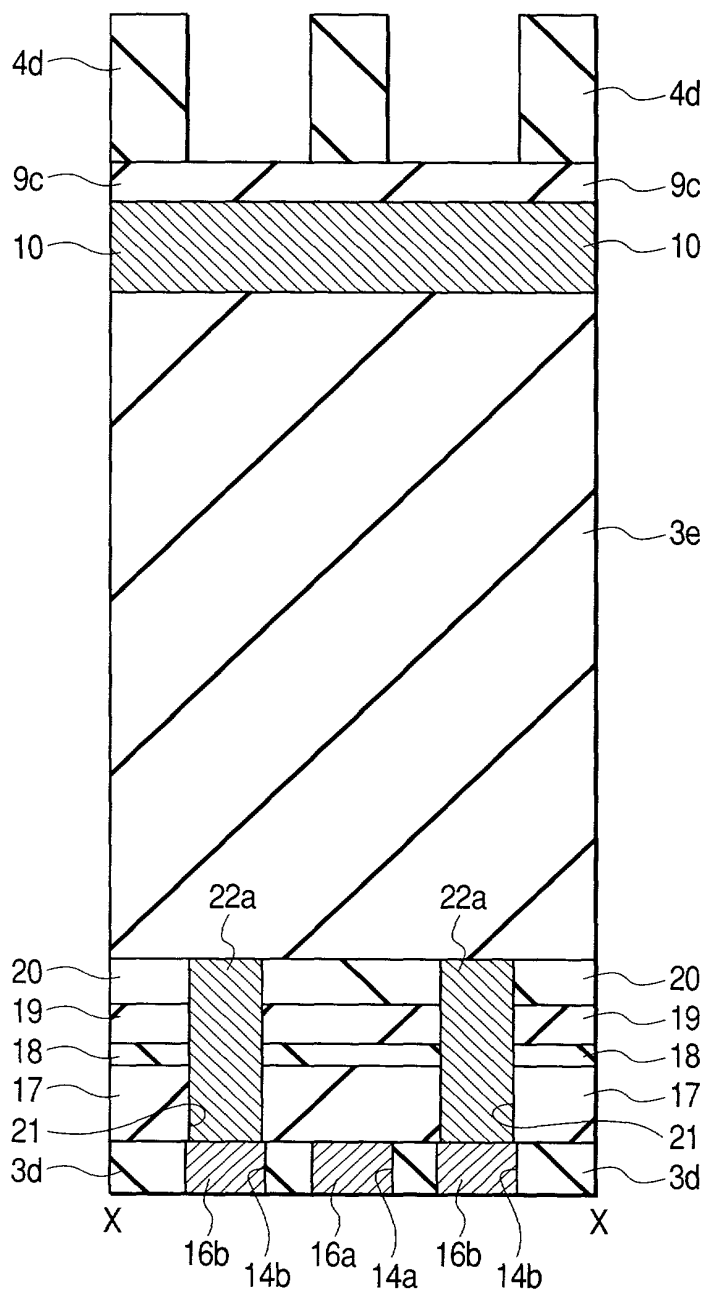


FIG. 32

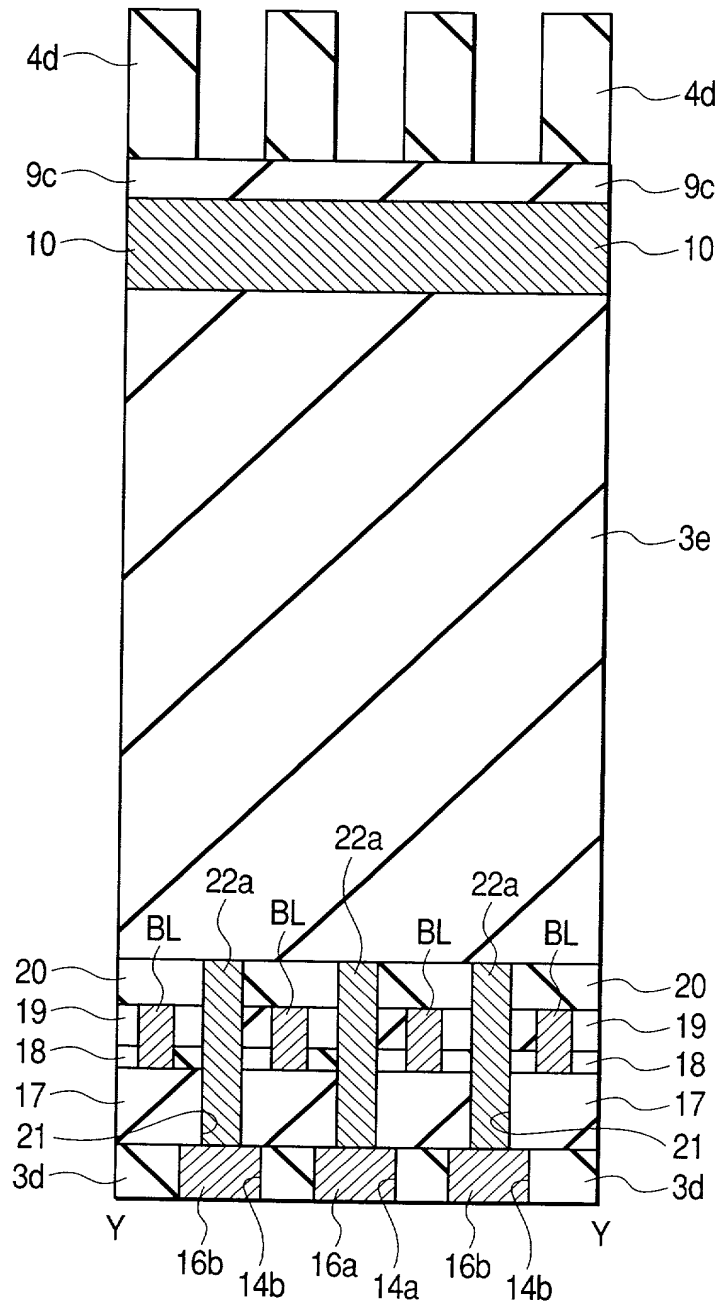


FIG. 33

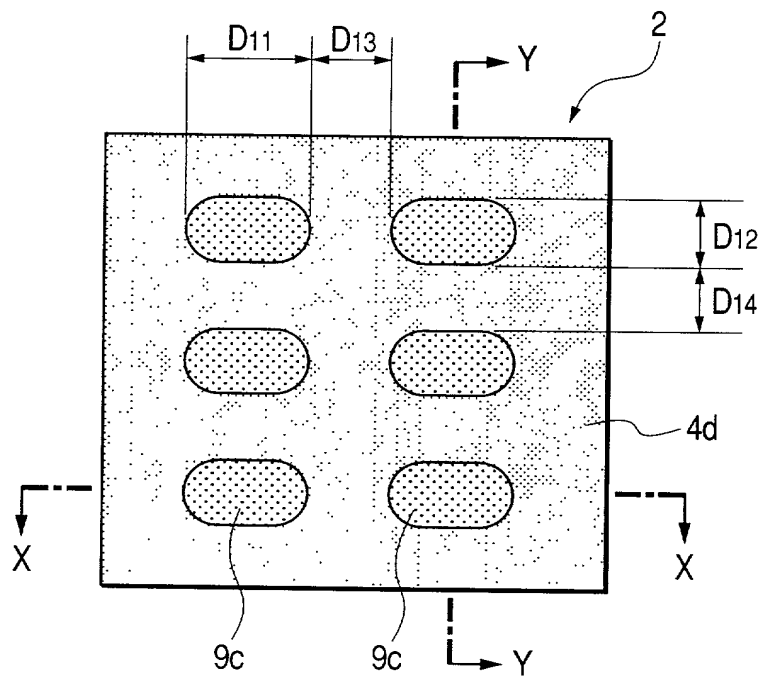


FIG. 34

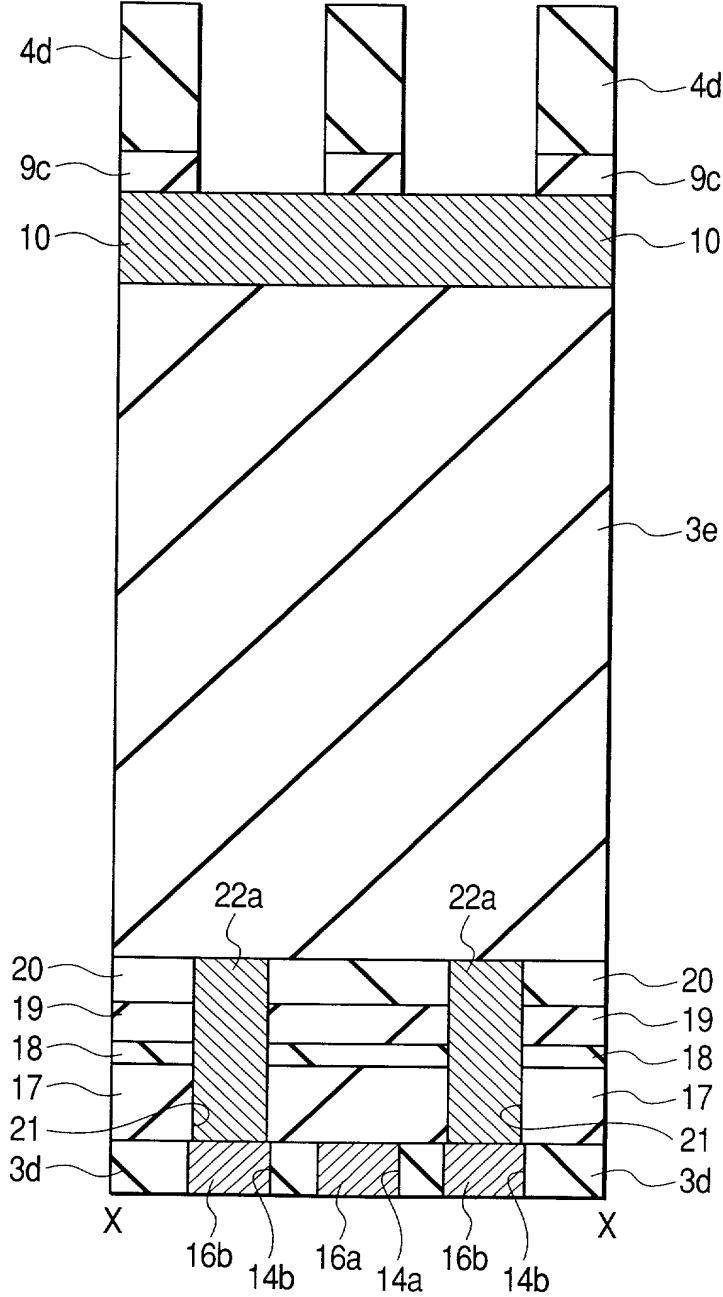


FIG. 35

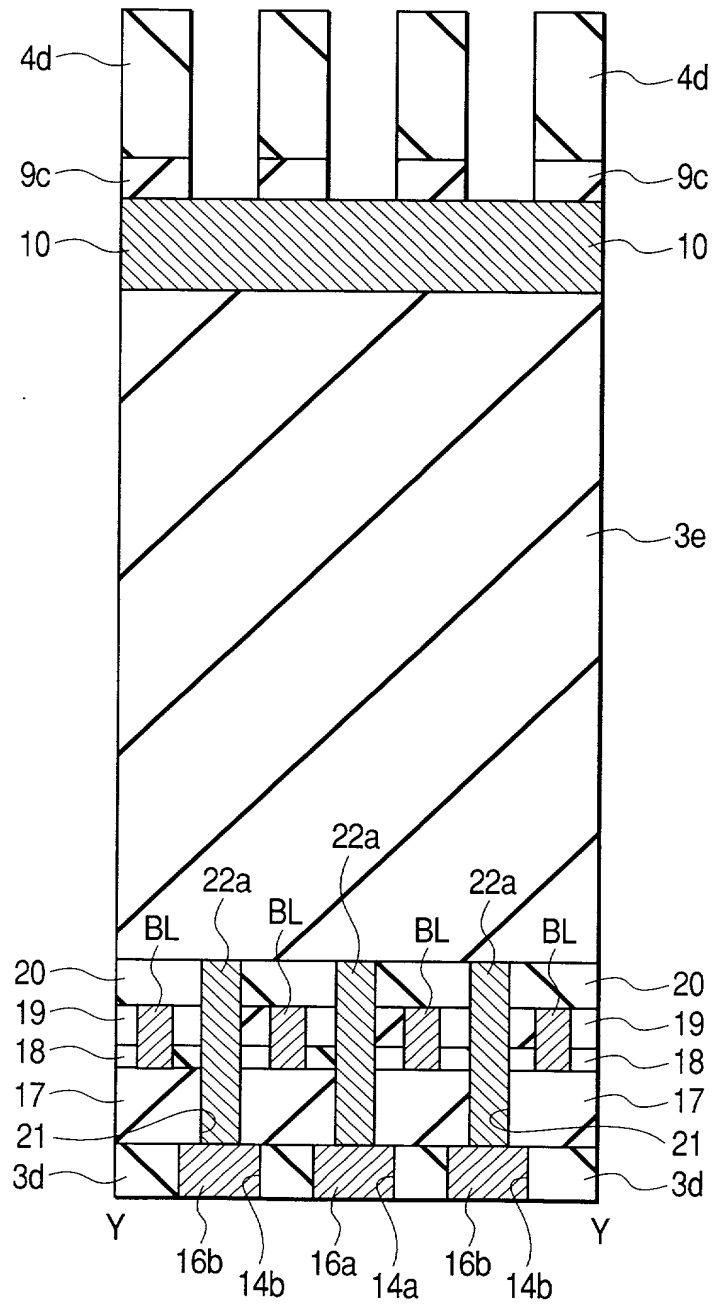


FIG. 36

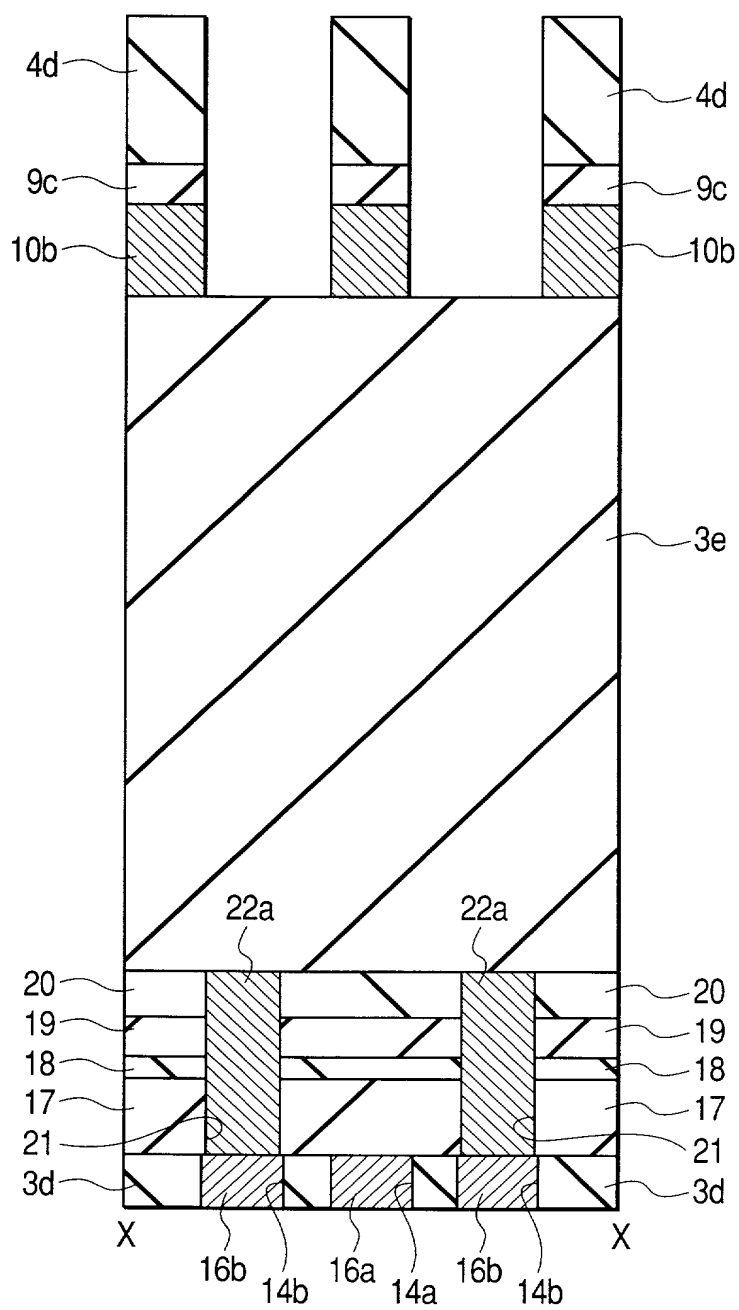


FIG. 37

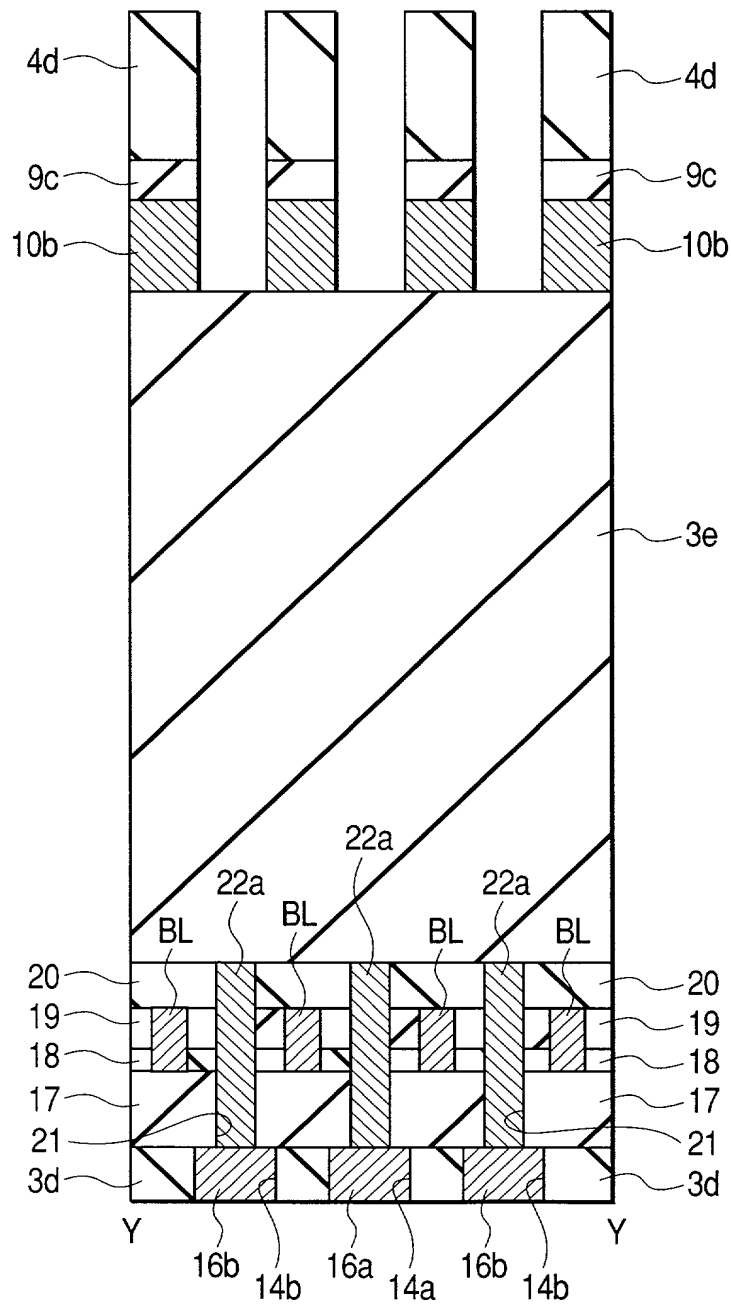


FIG. 38

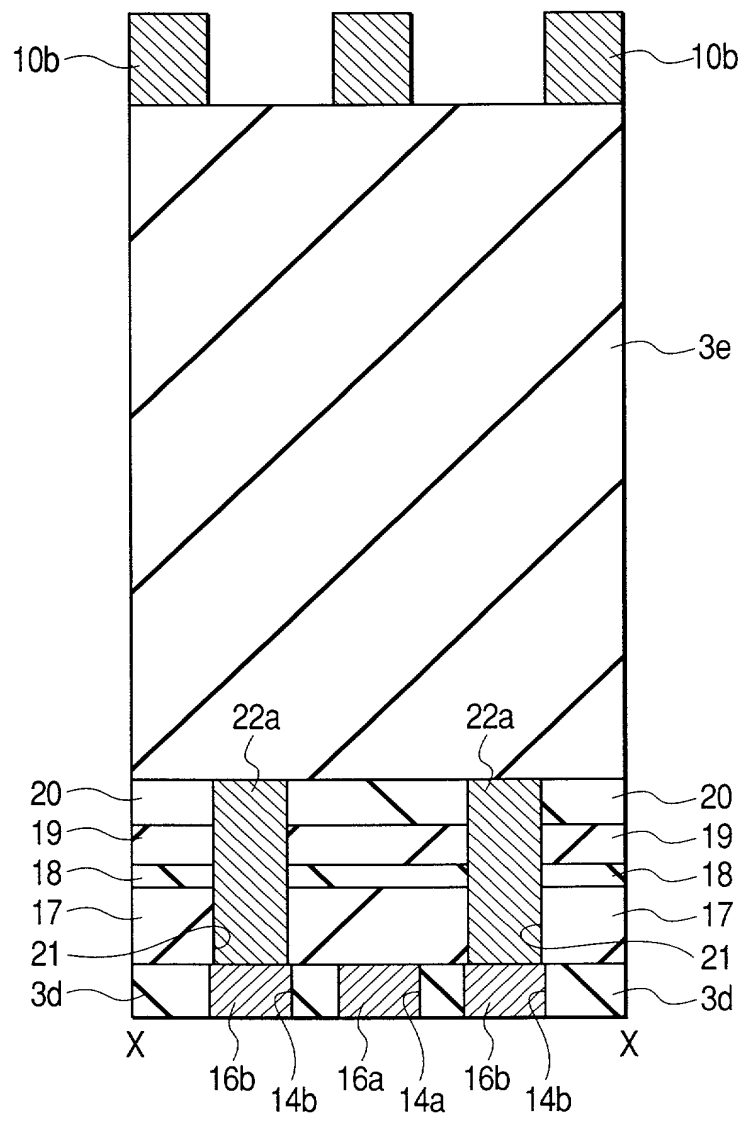


FIG. 39

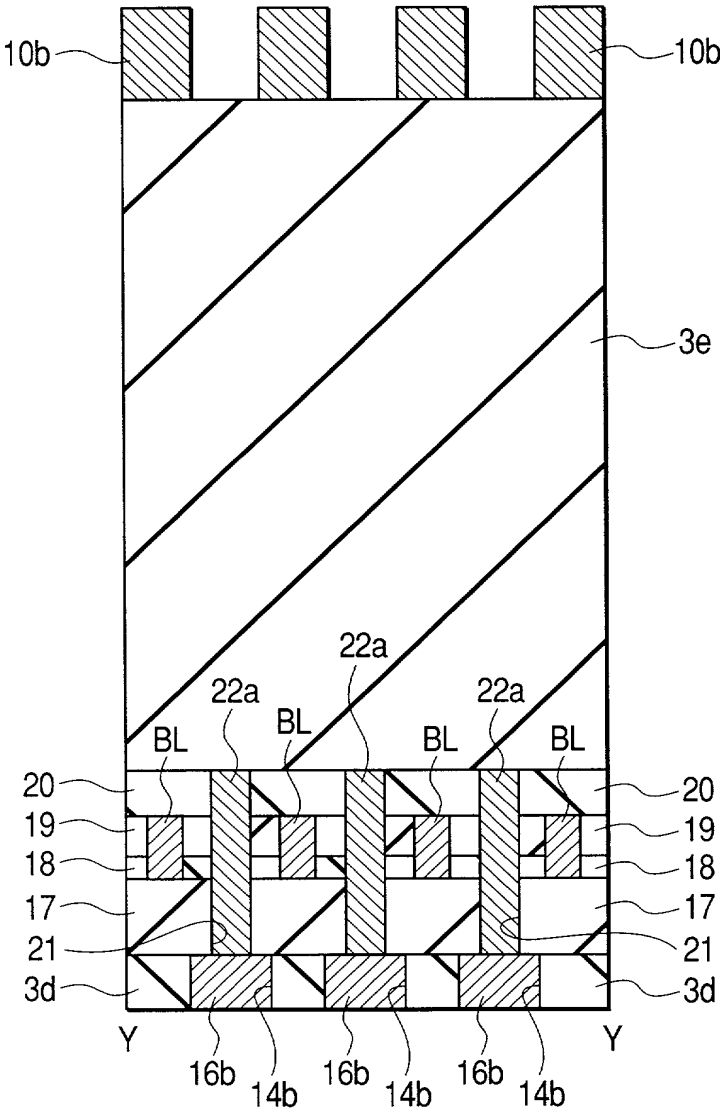
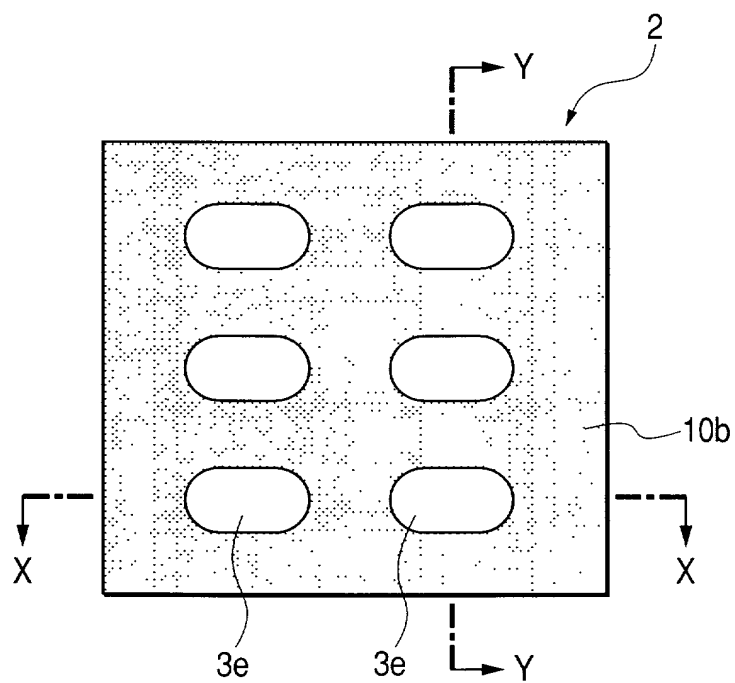


FIG. 40

This diagram shows a cross-sectional view of a semiconductor device. It features a series of vertical pillars (23) and a base structure (3d). The pillars are separated by spacers (22a) and have a central core (BL). The base structure includes layers 20, 19, 18, 17, 21, and 3d. The pillars are labeled 10b and 3e. The base structure is labeled Y, 16b, 14b, 16a, 14a, 16b, 14b, and Y.

FIG. 43

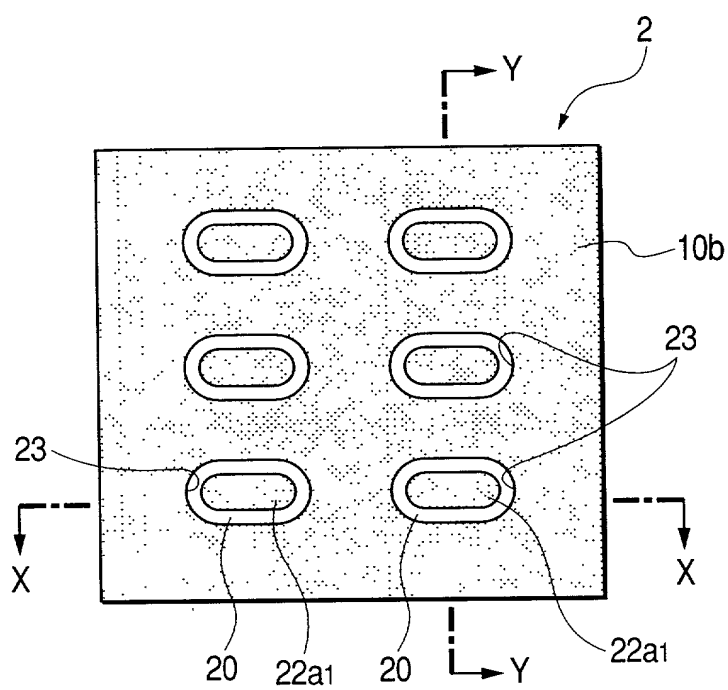


FIG. 44

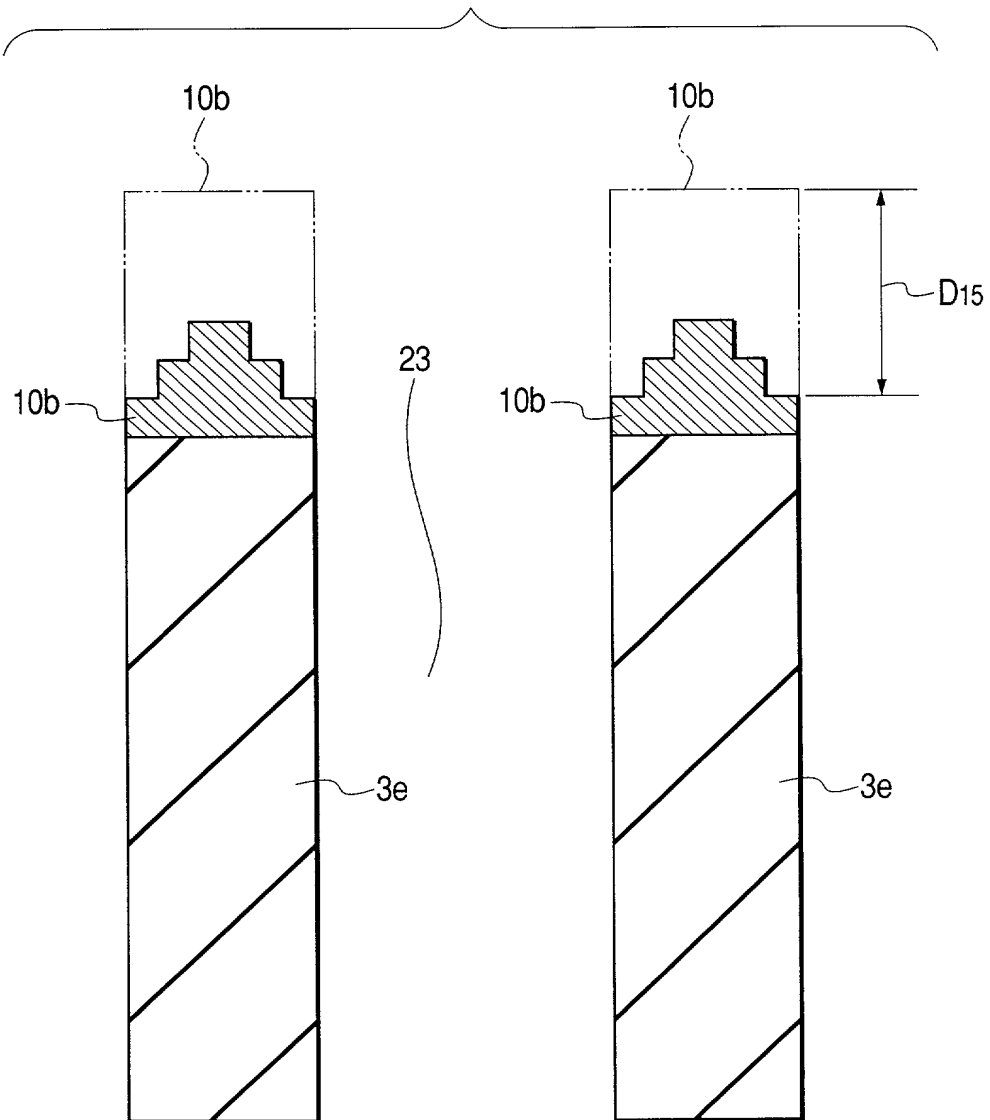


FIG. 45

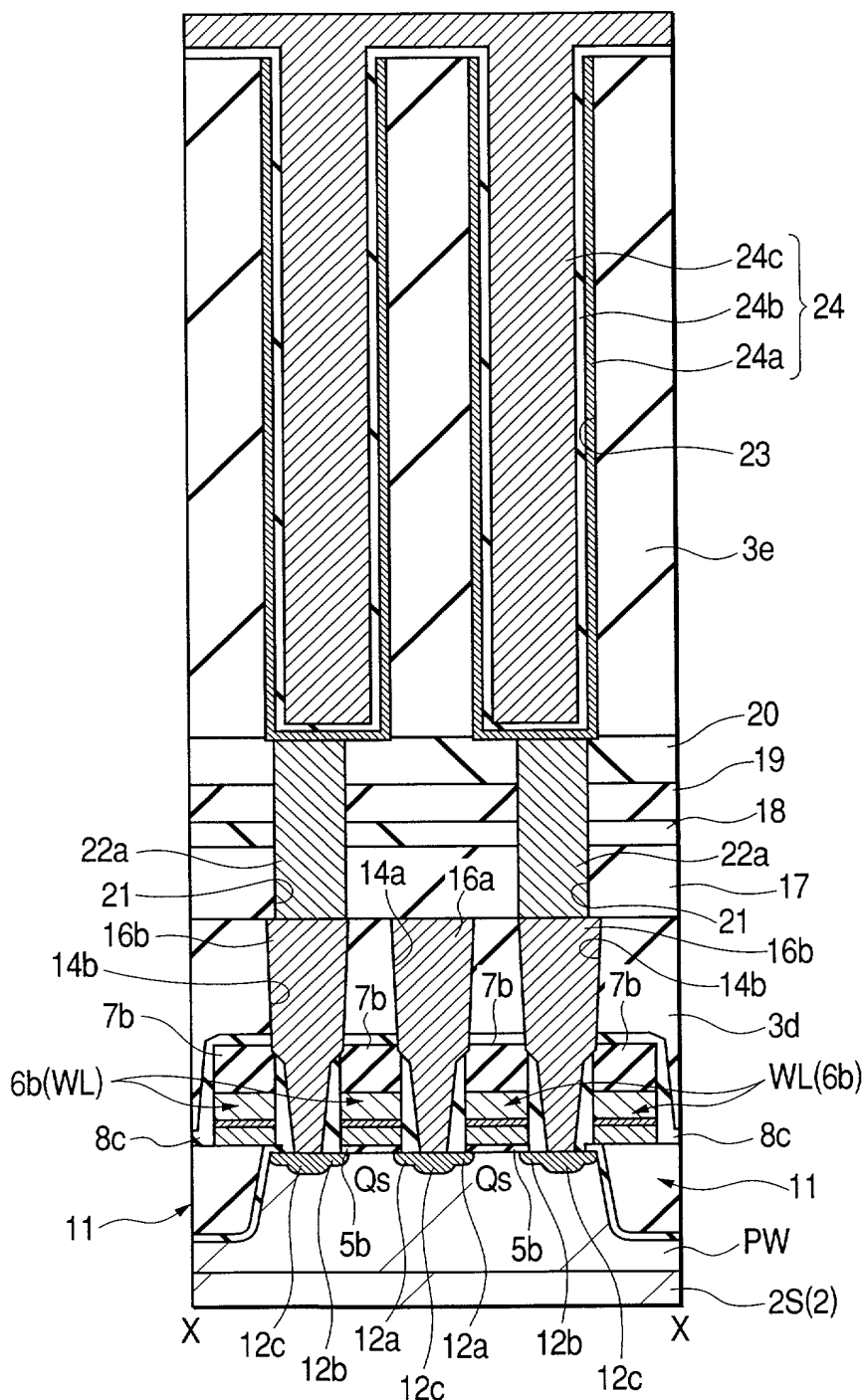


FIG. 46

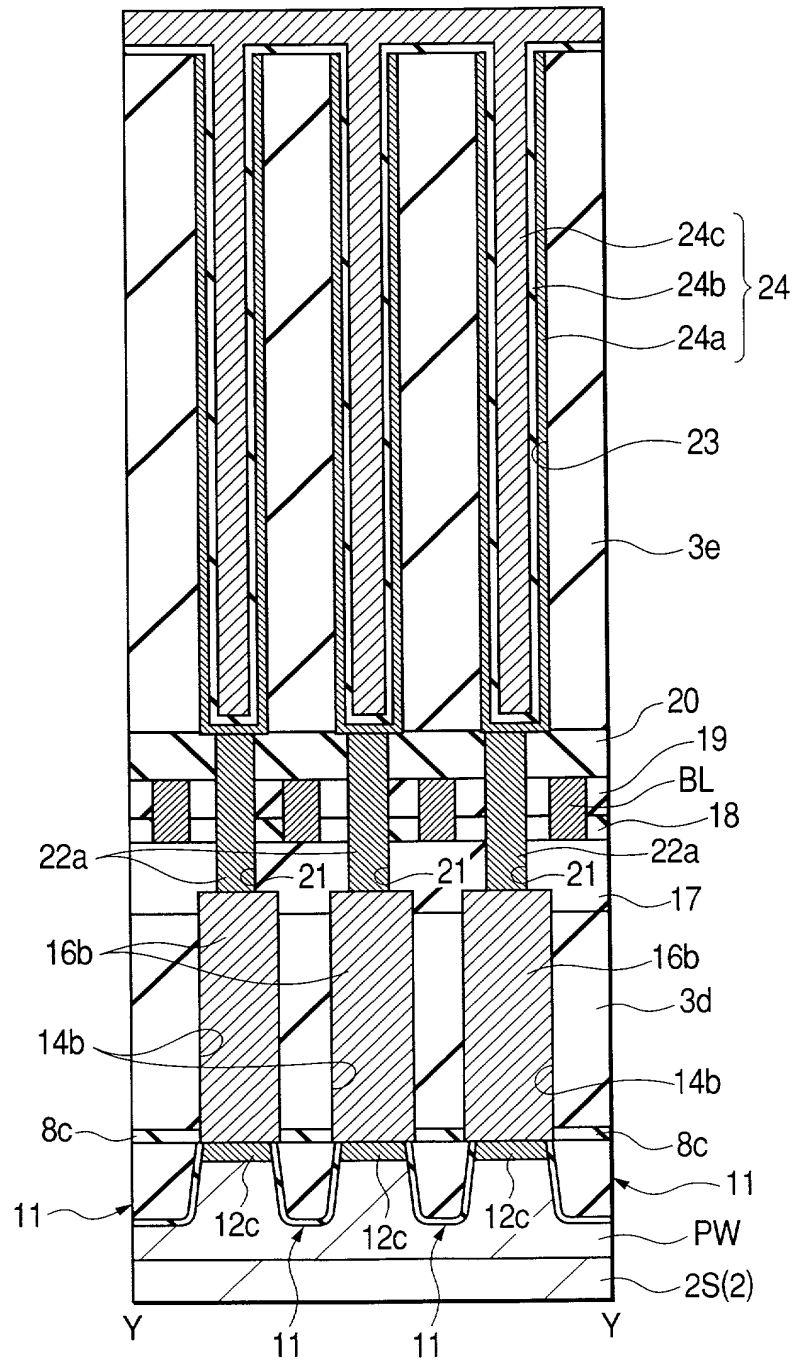


FIG. 47

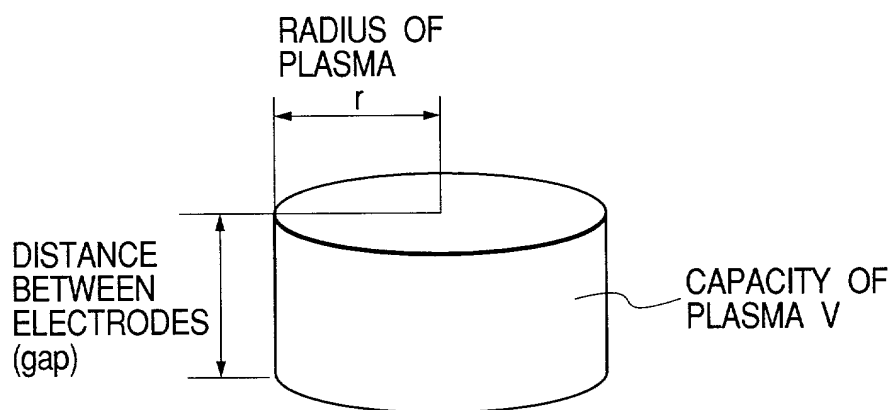


FIG. 48

